PNX2000 Register Summary List AN10276_1

Audio Video Input Processor

Rev. 01 — 15 December 2003

PHILIPS

RSL Contents

Aperture Map PNX2000

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Chapter 1: Overview

PNX2000 RSL

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1. Introduction

The RSL tables provide the following register information for PNX2000:

- Module name
- Offset address for each register with respect to module address
- Bitfield Summary (partitioning in fields of a simple register)
- Reset value of the register field
- Brief description of the register/bits

The following definitions apply:

Reserved - Bits are undefined and should not be written to.

Not Used - Bits can be written or read, but have no effect on any part of the PNX2000. **There is no guarantee that data written to these bits will be stored**.

The Aperture Map Table 1 includes the base address (Aperture Start) and reference page number for the PNX2000 registers. Registers are presented in numerical order by offset.

Table 1: Aperture Map PNX2000

Module Name	Aperture Start	Aperture Size	Page Reference
AUDIO_DSP	0x7f00000	256K	Table 1 on page 2-3
DCU	0x7ff5000	4K	Table 1 on page 3-73
DEMDEC_DSP	0x7f80000	256K	Table 1 on page 4-78
GPR	0x7ff7000	4K	Table 1 on page 5-98
I2D	0x7ff8000	4K	Table 1 on page 6-109
ITU656	0x7ffa000	4K	Table 1 on page 7-113
PI_1003_BCU	0x7fe8000	4K	Table 1 on page 8-119
VIDDEC	0x7ff9000	4K	Table 1 on page 9-121

Figure 1 shows the hierarchy of registers within PNX2000.

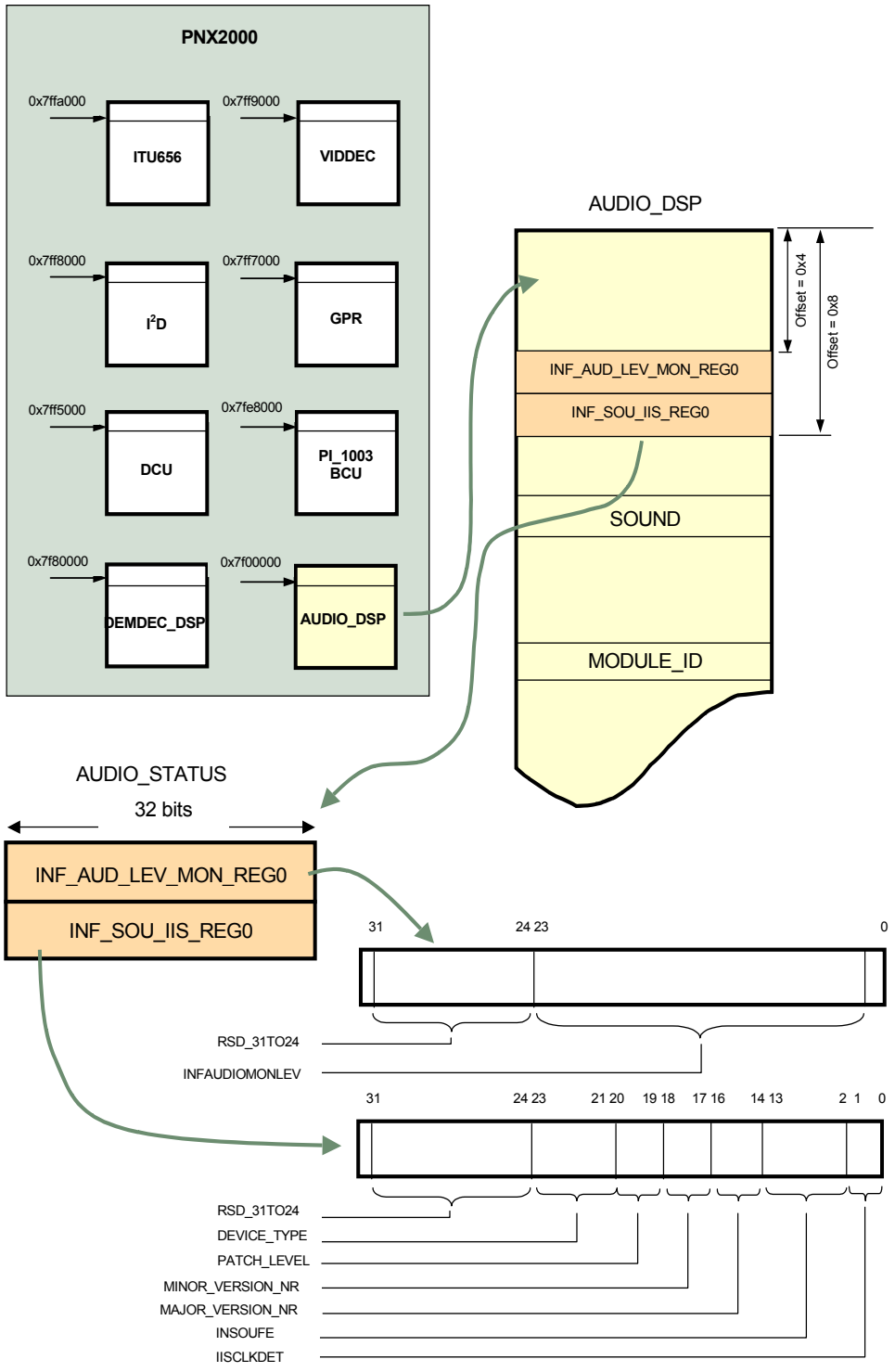

Figure 1: Register Hierarchy

Chapter 2: AUDIO_DSP Registers

PNX2000

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1. AUDIO_DSP Register Descriptions

Table 1: AUDIO_DSP Register Summary

Offset	Name	Description
0x4	INF_AUD_LEV_MON_REG0	
0x8	INF_SOU_IIS_REG0	
0xC	ASW_SUR_REG0	
0x10	ASW_MA_A1_A2_REG0	
0x14	ASW_A3_A4_REG0	
0x18	ASW_A5_A6_REG0	
0x1C	ASW_AFO1_4_REG0	
0x20	ASW_AFO5_8_REG0	
0x24	ASW_DAC1_2_REG0	
0x28	ASW_I2S1_2_REG0	
0x2C	ASW_I2S3_4_REG0	
0x30	ASW_I2S5_6_REG0	
0x34	ASW_MUT_CON_REG0	
0x38	LEV_ADJ_ADC_DEMDEC_IIS_REG0	
0x3C	LEV_ADJ_ADC_IIS_REG0	
0x40	LEV_ADJ_IIS3_4_5_6_REG0	
0x44	SOU_APP_MOD_REG0	
0x48	SOU_EFF_REG0	
0x4C	SOU_BASS_EFF_REG0	
0x50	DBE_COEF_DOWNL_REG0	
0x54	DUB_COEF_DOWNL_REG0	
0x58	DOL_CON_REG0	
0x5C	MAS_BEE_CON_REG0	
0x60	MAI_VOL_REG0	
0x64	SW_C_VOL_REG0	
0x68	LS_RS_VOL_REG0	
0x6C	A1_VOL_REG0	
0x70	A2_VOL_REG0	
0x74	A3_VOL_REG0	

Table 1: AUDIO_DSP Register Summary *...Continued*

Offset	Name	Description
0x78	A4_VOL_REG0	
0x7C	A5_VOL_REG0	
0x80	A6_VOL_REG0	
0x84	MAI_TON_CON_REG0	
0x88	CENTER_LFE_TON_CON_REG0	
0x8C	SURROUND_TON_CON_REG0	
0x90	AUX1_TON_CON_REG0	
0x94	EQ_CONFIG_REG0	
0x98	EQMAINBAND1_COEF_REG0	
0x9C	EQMAINBAND2_COEF_REG0	
0xA0	EQMAINBAND3_COEF_REG0	
0xA4	EQMAINBAND4_COEF_REG0	
0xA8	EQMAINBAND5_COEF_REG0	
0xAC	EQCENTERBAND1_COEF_REG0	
0xB0	EQCENTERBAND2_COEF_REG0	
0xB4	EQCENTERBAND3_COEF_REG0	
0xB8	EQCENTERBAND4_COEF_REG0	
0xBC	EQCENTERBAND5_COEF_REG0	
0xC0	EQMAIN1_TON_CON_REG0	
0xC4	EQMAIN2_TON_CON_REG0	
0xC8	EQCENTER1_TON_CON_REG0	
0xCC	EQCENTER2_TON_CON_REG0	
0xD0	MON_SEL_REG0	
0xD4	MPI_CONTROL_REG0	
0xD8	ACC_MAINCH_REG0	
0xDC	ACC_CENTERCH_REG0	
0xE0	AS_CONTROL_REG0	
0xE4	AS_PMC_TRIM_REG0	
0xE8	AS_IMONO_LFE_TRIM_REG0	
0xEC	AS_SIGNALSTATUS_REG0	
0xF0	AS_STATUS1_REG0	
0xF4	AS_STATUS2_REG0	
0xF8	DPL2_MM_CON_REG0	
0x180A8	SND_AD_STATUS00	
0x180B4	SND_AD_T020	
0x180B8	SND_AD_T010	
0x180BC	SND_AD_M000	
0x3FFE0	SND_AD_INT_STATUS0	

Table 1: AUDIO_DSP Register Summary *...Continued*

Offset	Name	Description
0x3FFE4	SND_AD_INT_ENABLE0	
0x3FFE8	SND_AD_INT_CLEAR0	
0x3FFEC	SND_AD_INT_SET0	
0x3FFFC	SND_AD_MOD_ID0	

Table 2: AUDIO_DSP Registers

Bit	Symbol	Access	Reset Value	Description
Offset 0x4	***INF_AUD_LEV_MON_REG0***			
23:0	INFAUDIOMONLEV	R	0x000000	Audio Monitor level register
Offset 0x8	***INF_SOU_IIS_REG0***			
1:0	IISCLKDET	R	0x0	Sample rate detector info 0: V0; 32 kHz (6-38 kHz) 1: V1; 44.1 kHz (38-46 kHz) 10: V2; 48 kHz (> 46 kHz) 11: V3; < 6 kHz
13:2	INFSOUFE	R	0x000	Information which sound feature will be available. (DPL, VDS, equalizer, MAIN, AUX1/SW, AUX2/C,Ä)
16:14	MAJOR_VERSION_NR	R	0x0	major version number. incremented number means: control interface has major changes w.r.t lower number. driver update required or strongly recommended.
18:17	MINOR_VERSION_NR	R	0x0	minor version number. incremented number means: control interface may have extensions for additional functions or functionality may have changed slightly; driver update recommended.
20:19	PATCH_LEVEL	R	0x0	patch level number. incremented number indicates bugfixes of the embedded software without any change of control interface or functionality. no driver update needed.
23:21	DEVICE_TYPE	R	0x0	device type, gives the PNX2000 hardware version which should be used.

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
Offset 0xC	***ASW_SUR_REG0***			
4:0	CINSS	R/W	0x08	SIGNAL SOURCE CENTER 0: V00; DecL 1: V01; DecR 10: V02; Mono 11: V03; SAP 100: V04; PIPMono 101: V05; Adc1L 110: V06; Adc1R 111: V07; Noise 1000: V08; silence 1001: V09; MonC1 1010: V0A; MonC2 1011: V0B; IIS11 1100: V0C; IIS12 1101: V0D; IIS21 1110: V0E; IIS22 1111: V0F; IIS31 0x10: V10; IIS32 0x11: V11; IIS41 0x12: V12; IIS42 0x13: V13; IIS51 0x14: V14; IIS52 0x15: V15; IIS61 0x16: V16; IIS62 0x17: V17; Reserved 0x18: V18; Reserved 0x19: V19; Reserved 0x1A: V1A; Reserved 0x1B: V1B; Reserved 0x1C: V1C; Reserved 0x1D: V1D; Reserved 0x1E: V1E; Reserved 0x1F: V1F; Reserved

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
9:5	SLINSS	R/W	0x08	SIGNAL SOURCE Ls 0: V00; DecL 1: V01; DecR 10: V02; Mono 11: V03; SAP 100: V04; PIPMono 101: V05; Adc1L 110: V06; Adc1R 111: V07; Noise 1000: V08; silence 1001: V09; MonC1 1010: V0A; MonC2 1011: V0B; IIS11 1100: V0C; IIS12 1101: V0D; IIS21 1110: V0E; IIS22 1111: V0F; IIS31 0x10: V10; IIS32 0x11: V11; IIS41 0x12: V12; IIS42 0x13: V13; IIS51 0x14: V14; IIS52 0x15: V15; IIS61 0x16: V16; IIS62 0x17: V17; Reserved 0x18: V18; Reserved 0x19: V19; Reserved 0x1A: V1A; Reserved 0x1B: V1B; Reserved 0x1C: V1C; Reserved 0x1D: V1D; Reserved 0x1E: V1E; Reserved 0x1F: V1F; Reserved

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
14:10	SRINSS	R/W	0x08	SIGNAL SOURCE Rs 0: V00; DecL 1: V01; DecR 10: V02; Mono 11: V03; SAP 100: V04; PIPMono 101: V05; Adc1L 110: V06; Adc1R 111: V07; Noise 1000: V08; silence 1001: V09; MonC1 1010: V0A; MonC2 1011: V0B; IIS11 1100: V0C; IIS12 1101: V0D; IIS21 1110: V0E; IIS22 1111: V0F; IIS31 0x10: V10; IIS32 0x11: V11; IIS41 0x12: V12; IIS42 0x13: V13; IIS51 0x14: V14; IIS52 0x15: V15; IIS61 0x16: V16; IIS62 0x17: V17; Reserved 0x18: V18; Reserved 0x19: V19; Reserved 0x1A: V1A; Reserved 0x1B: V1B; Reserved 0x1C: V1C; Reserved 0x1D: V1D; Reserved 0x1E: V1E; Reserved 0x1F: V1F; Reserved

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
19:15	LFEINSS	R/W	0x08	SIGNAL SOURCE LFE 0: V00; DecL 1: V01; DecR 10: V02; Mono 11: V03; SAP 100: V04; PIPMono 101: V05; Adc1L 110: V06; Adc1R 111: V07; Noise 1000: V08; silence 1001: V09; MonC1 1010: V0A; MonC2 1011: V0B; IIS11 1100: V0C; IIS12 1101: V0D; IIS21 1110: V0E; IIS22 1111: V0F; IIS31 0x10: V10; IIS32 0x11: V11; IIS41 0x12: V12; IIS42 0x13: V13; IIS51 0x14: V14; IIS52 0x15: V15; IIS61 0x16: V16; IIS62 0x17: V17; Reserved 0x18: V18; Reserved 0x19: V19; Reserved 0x1A: V1A; Reserved 0x1B: V1B; Reserved 0x1C: V1C; Reserved 0x1D: V1D; Reserved 0x1E: V1E; Reserved 0x1F: V1F; Reserved
23:20	RSD_23To20	R/W	0x0	0

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
Offset 0x10	***ASW_MA_A1_A2_REG0***			
4:0	MAINSS	R/W	0x00	SIGNAL SOURCE MAIN 0: V00; DEC 1: V01; Mono 10: V02; SAP 11: V03; PIPMONO 100: V04; ADC1 101: V05; Noise Generator 110: V06; Outcopy 111: V07; IIS 1.1 1.2 1000: V08; IIS 1.1 2.1 1001: V09; IIS 1.1 2.2 1010: V0A; IIS 1.1 3.1 1011: V0B; IIS 1.1 3.2 1100: V0C; IIS 1.1 4.1 1101: V0D; IIS 1.1 4.2 1110: V0E; IIS 1.2 2.1 1111: V0F; IIS 1.2 2.2 0x10: V10; IIS 1.2 3.1 0x11: V11; IIS 1.2 3.2 0x12: V12; IIS 1.2 4.1 0x13: V13; IIS 1.2 4.2 0x14: V14; IIS 2.1 2.2 0x15: V15; IIS 2.1 3.1 0x16: V16; IIS 2.1 3.2 0x17: V17; IIS 2.2 3.1 0x18: V18; IIS 2.2 3.2 0x19: V19; IIS 3.1 3.2 0x1A: V1A; IIS 4.1 4.2 0x1B: V1B; IIS 5.1 5.2 0x1C: V1C; IIS 6.1 6.2 0x1D: V1D; Digital Silence 0x1E: V1E; Reserved 0x1F: V1F; Reserved
7:5	MAINDM	R/W	0x0	DIGITAL MATRIX MAIN 0: V0; AB [Stereo] (automatrix off) 1: V1; (A+B)/2 [Mono] (automatrix off) 10: V2; AA [Lang. A] (automatrix off) 11: V3; BB [Lang. B] (automatrix off) 100: V4; BA [Swap] (automatrix off) 101: V5; Reserved 110: V6; Language A (automatrix on) 111: V7; Language B (automatrix on)

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
12:8	AUX1SS	R/W	0x00	SIGNAL SOURCE AUX1/HP 0: V00; DEC 1: V01; Mono 10: V02; SAP 11: V03; PIPMONO 100: V04; ADC1 101: V05; Noise Generator 110: V06; Outcopy 111: V07; IIS 1.1 1.2 1000: V08; IIS 1.1 2.1 1001: V09; IIS 1.1 2.2 1010: V0A; IIS 1.1 3.1 1011: V0B; IIS 1.1 3.2 1100: V0C; IIS 1.1 4.1 1101: V0D; IIS 1.1 4.2 1110: V0E; IIS 1.2 2.1 1111: V0F; IIS 1.2 2.2 0x10: V10; IIS 1.2 3.1 0x11: V11; IIS 1.2 3.2 0x12: V12; IIS 1.2 4.1 0x13: V13; IIS 1.2 4.2 0x14: V14; IIS 2.1 2.2 0x15: V15; IIS 2.1 3.1 0x16: V16; IIS 2.1 3.2 0x17: V17; IIS 2.2 3.1 0x18: V18; IIS 2.2 3.2 0x19: V19; IIS 3.1 3.2 0x1A: V1A; IIS 4.1 4.2 0x1B: V1B; IIS 5.1 5.2 0x1C: V1C; IIS 6.1 6.2 0x1D: V1D; Digital Silence 0x1E: V1E; Reserved 0x1F: V1F; Reserved
15:13	AUX1DM	R/W	0x0	DIGITAL MATRIX AUX1/HP 0: V0; AB [Stereo] (automatrix off) 1: V1; (A+B)/2 [Mono] (automatrix off) 10: V2; AA [Lang. A] (automatrix off) 11: V3; BB [Lang. B] (automatrix off) 100: V4; BA [Swap] (automatrix off) 101: V5; Reserved 110: V6; Language A (automatrix on) 111: V7; Language B (automatrix on)

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
20:16	AUX2SS	R/W	0x00	SIGNAL SOURCE AUX2/IIS1 0: V00; DEC 1: V01; Mono 10: V02; SAP 11: V03; PIPMONO 100: V04; ADC1 101: V05; Noise Generator 110: V06; Outcopy 111: V07; IIS 1.1 1.2 1000: V08; IIS 1.1 2.1 1001: V09; IIS 1.1 2.2 1010: V0A; IIS 1.1 3.1 1011: V0B; IIS 1.1 3.2 1100: V0C; IIS 1.1 4.1 1101: V0D; IIS 1.1 4.2 1110: V0E; IIS 1.2 2.1 1111: V0F; IIS 1.2 2.2 0x10: V10; IIS 1.2 3.1 0x11: V11; IIS 1.2 3.2 0x12: V12; IIS 1.2 4.1 0x13: V13; IIS 1.2 4.2 0x14: V14; IIS 2.1 2.2 0x15: V15; IIS 2.1 3.1 0x16: V16; IIS 2.1 3.2 0x17: V17; IIS 2.2 3.1 0x18: V18; IIS 2.2 3.2 0x19: V19; IIS 3.1 3.2 0x1A: V1A; IIS 4.1 4.2 0x1B: V1B; IIS 5.1 5.2 0x1C: V1C; IIS 6.1 6.2 0x1D: V1D; Digital Silence 0x1E: V1E; Reserved 0x1F: V1F; Reserved
23:21	AUX2DM	R/W	0x0	DIGITAL MATRIX AUX2/IIS1 0: V0; AB [Stereo] (automatrix off) 1: V1; (A+B)/2 [Mono] (automatrix off) 10: V2; AA [Lang. A] (automatrix off) 11: V3; BB [Lang. B] (automatrix off) 100: V4; BA [Swap] (automatrix off) 101: V5; Reserved 110: V6; Language A (automatrix on) 111: V7; Language B (automatrix on)

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
Offset 0x14	***ASW_A3_A4_REG0***			
4:0	AUX3SS	R/W	0x00	SIGNAL SOURCE AUX3/IIS2 0: V00; DEC 1: V01; Mono 10: V02; SAP 11: V03; PIPMONO 100: V04; ADC1 101: V05; Noise Generator 110: V06; Outcopy 111: V07; IIS 1.1 1.2 1000: V08; IIS 1.1 2.1 1001: V09; IIS 1.1 2.2 1010: V0A; IIS 1.1 3.1 1011: V0B; IIS 1.1 3.2 1100: V0C; IIS 1.1 4.1 1101: V0D; IIS 1.1 4.2 1110: V0E; IIS 1.2 2.1 1111: V0F; IIS 1.2 2.2 0x10: V10; IIS 1.2 3.1 0x11: V11; IIS 1.2 3.2 0x12: V12; IIS 1.2 4.1 0x13: V13; IIS 1.2 4.2 0x14: V14; IIS 2.1 2.2 0x15: V15; IIS 2.1 3.1 0x16: V16; IIS 2.1 3.2 0x17: V17; IIS 2.2 3.1 0x18: V18; IIS 2.2 3.2 0x19: V19; IIS 3.1 3.2 0x1A: V1A; IIS 4.1 4.2 0x1B: V1B; IIS 5.1 5.2 0x1C: V1C; IIS 6.1 6.2 0x1D: V1D; Digital Silence 0x1E: V1E; Reserved 0x1F: V1F; Reserved
7:5	AUX3DM	R/W	0x0	DIGITAL MATRIX AUX3/IIS2 0: V0; AB [Stereo] (automatrix off) 1: V1; (A+B)/2 [Mono] (automatrix off) 10: V2; AA [Lang. A] (automatrix off) 11: V3; BB [Lang. B] (automatrix off) 100: V4; BA [Swap] (automatrix off) 101: V5; Reserved 110: V6; Language A (automatrix on) 111: V7; Language B (automatrix on)

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
12:8	AUX4SS	R/W	0x00	SIGNAL SOURCE AUX4 0: V00; DEC 1: V01; Mono 10: V02; SAP 11: V03; PIPMONO 100: V04; ADC1 101: V05; Noise Generator 110: V06; Outcopy 111: V07; IIS 1.1 1.2 1000: V08; IIS 1.1 2.1 1001: V09; IIS 1.1 2.2 1010: V0A; IIS 1.1 3.1 1011: V0B; IIS 1.1 3.2 1100: V0C; IIS 1.1 4.1 1101: V0D; IIS 1.1 4.2 1110: V0E; IIS 1.2 2.1 1111: V0F; IIS 1.2 2.2 0x10: V10; IIS 1.2 3.1 0x11: V11; IIS 1.2 3.2 0x12: V12; IIS 1.2 4.1 0x13: V13; IIS 1.2 4.2 0x14: V14; IIS 2.1 2.2 0x15: V15; IIS 2.1 3.1 0x16: V16; IIS 2.1 3.2 0x17: V17; IIS 2.2 3.1 0x18: V18; IIS 2.2 3.2 0x19: V19; IIS 3.1 3.2 0x1A: V1A; IIS 4.1 4.2 0x1B: V1B; IIS 5.1 5.2 0x1C: V1C; IIS 6.1 6.2 0x1D: V1D; Digital Silence 0x1E: V1E; Reserved 0x1F: V1F; Reserved
15:13	AUX4DM	R/W	0x0	DIGITAL MATRIX AUX4 0: V0; AB [Stereo] (automatrix off) 1: V1; (A+B)/2 [Mono] (automatrix off) 10: V2; AA [Lang. A] (automatrix off) 11: V3; BB [Lang. B] (automatrix off) 100: V4; BA [Swap] (automatrix off) 101: V5; Reserved 110: V6; Language A (automatrix on) 111: V7; Language B (automatrix on)
23:16	RSD_23To16	R/W	0x00	Not used, must be fixed to '0'

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
Offset 0x18	***ASW_A5_A6_REG0***			
4:0	AUX5SS	R/W	0x00	SIGNAL SOURCE AUX5/DAC1 0: V00; DEC 1: V01; Mono 10: V02; SAP 11: V03; PIPMONO 100: V04; ADC1 101: V05; Noise Generator 110: V06; Outcopy 111: V07; IIS 1.1 1.2 1000: V08; IIS 1.1 2.1 1001: V09; IIS 1.1 2.2 1010: V0A; IIS 1.1 3.1 1011: V0B; IIS 1.1 3.2 1100: V0C; IIS 1.1 4.1 1101: V0D; IIS 1.1 4.2 1110: V0E; IIS 1.2 2.1 1111: V0F; IIS 1.2 2.2 0x10: V10; IIS 1.2 3.1 0x11: V11; IIS 1.2 3.2 0x12: V12; IIS 1.2 4.1 0x13: V13; IIS 1.2 4.2 0x14: V14; IIS 2.1 2.2 0x15: V15; IIS 2.1 3.1 0x16: V16; IIS 2.1 3.2 0x17: V17; IIS 2.2 3.1 0x18: V18; IIS 2.2 3.2 0x19: V19; IIS 3.1 3.2 0x1A: V1A; IIS 4.1 4.2 0x1B: V1B; IIS 5.1 5.2 0x1C: V1C; IIS 6.1 6.2 0x1D: V1D; Digital Silence 0x1E: V1E; Reserved 0x1F: V1F; Reserved
7:5	AUX5DM	R/W	0x0	DIGITAL MATRIX AUX5/DAC1 0: V0; AB [Stereo] (automatrix off) 1: V1; (A+B)/2 [Mono] (automatrix off) 10: V2; AA [Lang. A] (automatrix off) 11: V3; BB [Lang. B] (automatrix off) 100: V4; BA [Swap] (automatrix off) 101: V5; Reserved 110: V6; Language A (automatrix on) 111: V7; Language B (automatrix on)

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
12:8	AUX6SS	R/W	0x00	SIGNAL SOURCE AUX6/DAC2 0: V00; DEC 1: V01; Mono 10: V02; SAP 11: V03; PIPMONO 100: V04; ADC1 101: V05; Noise Generator 110: V06; Outcopy 111: V07; IIS 1.1 1.2 1000: V08; IIS 1.1 2.1 1001: V09; IIS 1.1 2.2 1010: V0A; IIS 1.1 3.1 1011: V0B; IIS 1.1 3.2 1100: V0C; IIS 1.1 4.1 1101: V0D; IIS 1.1 4.2 1110: V0E; IIS 1.2 2.1 1111: V0F; IIS 1.2 2.2 0x10: V10; IIS 1.2 3.1 0x11: V11; IIS 1.2 3.2 0x12: V12; IIS 1.2 4.1 0x13: V13; IIS 1.2 4.2 0x14: V14; IIS 2.1 2.2 0x15: V15; IIS 2.1 3.1 0x16: V16; IIS 2.1 3.2 0x17: V17; IIS 2.2 3.1 0x18: V18; IIS 2.2 3.2 0x19: V19; IIS 3.1 3.2 0x1A: V1A; IIS 4.1 4.2 0x1B: V1B; IIS 5.1 5.2 0x1C: V1C; IIS 6.1 6.2 0x1D: V1D; Digital Silence 0x1E: V1E; Reserved 0x1F: V1F; Reserved
15:13	AUX6DM	R/W	0x0	DIGITAL MATRIX AUX6/DAC2 0: V0; AB [Stereo] (automatrix off) 1: V1; (A+B)/2 [Mono] (automatrix off) 10: V2; AA [Lang. A] (automatrix off) 11: V3; BB [Lang. B] (automatrix off) 100: V4; BA [Swap] (automatrix off) 101: V5; Reserved 110: V6; Language A (automatrix on) 111: V7; Language B (automatrix on)
23:16	RSD_23To16	R/W	0x00	Not used, must be fixed to '0'

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
Offset 0x1C	***ASW_AFO1_4_REG0***			
4:0	ASAFO1	R/W	0x00	OUTPUT SELECTION for DAFO1 $0 = MAIN/L CHANNEL $1 = MAIN/R CHANNEL $2 = SUB CHANNEL $3 = C CHANNEL $4 = SL CHANNEL $5 = SR CHANNEL $6 = AUX1L CHANNEL $7 = AUX1R CHANNEL $8 = AUX2L CHANNEL $9 = AUX2R CHANNEL $A = AUX3L CHANNEL $B = AUX3R CHANNEL $C = AUX4L CHANNEL $D = AUX4R CHANNEL $E = AUX5 L CHANNEL $F = AUX5 R CHANNEL $10 = AUX6 L CHANNEL $11 = AUX6 R CHANNEL $12 = Main Sum CHANNEL >$12 = reserved 0: V0; MAIN/L CHANNEL 1: V1; MAIN/R CHANNEL 10: V2; SUB CHANNEL 11: V3; C CHANNEL 100: V4; SL CHANNEL 101: V5; SR CHANNEL 110: V6; AUX1L CHANNEL 111: V7; AUX1R CHANNEL 1000: V8; AUX2L CHANNEL 1001: V9; AUX2R CHANNEL 1010: VA; AUX3L CHANNEL 1011: VB; AUX3R CHANNEL 1100: VC; AUX4L CHANNEL 1101: VD; AUX4R CHANNEL 1110: VE; AUX5 L CHANNEL 1111: VF; AUX5 R CHANNEL 0x10: V10; AUX6 L CHANNEL 0x11: V11; AUX6 R CHANNEL 0x12: V12; Main Sum CHANNEL

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
9:5	ASAFO2	R/W	0x01	OUTPUT SELECTION for DAFO2 $0 = MAIN/L CHANNEL $1 = MAIN/R CHANNEL $2 = SUB CHANNEL $3 = C CHANNEL $4 = SL CHANNEL $5 = SR CHANNEL $6 = AUX1L CHANNEL $7 = AUX1R CHANNEL $8 = AUX2L CHANNEL $9 = AUX2R CHANNEL $A = AUX3L CHANNEL $B = AUX3R CHANNEL $C = AUX4L CHANNEL $D = AUX4R CHANNEL $E = AUX5 L CHANNEL $F = AUX5 R CHANNEL $10 = AUX6 L CHANNEL $11 = AUX6 R CHANNEL $12 = Main Sum CHANNEL >$12 = reserved 0: V0; MAIN/L CHANNEL 1: V1; MAIN/R CHANNEL 10: V2; SUB CHANNEL 11: V3; C CHANNEL 100: V4; SL CHANNEL 101: V5; SR CHANNEL 110: V6; AUX1L CHANNEL 111: V7; AUX1R CHANNEL 1000: V8; AUX2L CHANNEL 1001: V9; AUX2R CHANNEL 1010: VA; AUX3L CHANNEL 1011: VB; AUX3R CHANNEL 1100: VC; AUX4L CHANNEL 1101: VD; AUX4R CHANNEL 1110: VE; AUX5 L CHANNEL 1111: VF; AUX5 R CHANNEL 0x10: V10; AUX6 L CHANNEL 0x11: V11; AUX6 R CHANNEL 0x12: V12; Main Sum CHANNEL

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
14:10	ASAFO3	R/W	0x02	OUTPUT SELECTION for DAFO3 $0 = MAIN/L CHANNEL $1 = MAIN/R CHANNEL $2 = SUB CHANNEL $3 = C CHANNEL $4 = SL CHANNEL $5 = SR CHANNEL $6 = AUX1L CHANNEL $7 = AUX1R CHANNEL $8 = AUX2L CHANNEL $9 = AUX2R CHANNEL $A = AUX3L CHANNEL $B = AUX3R CHANNEL $C = AUX4L CHANNEL $D = AUX4R CHANNEL $E = AUX5 L CHANNEL $F = AUX5 R CHANNEL $10 = AUX6 L CHANNEL $11 = AUX6 R CHANNEL $12 = Main Sum CHANNEL >$12 = reserved 0: V0; MAIN/L CHANNEL 1: V1; MAIN/R CHANNEL 10: V2; SUB CHANNEL 11: V3; C CHANNEL 100: V4; SL CHANNEL 101: V5; SR CHANNEL 110: V6; AUX1L CHANNEL 111: V7; AUX1R CHANNEL 1000: V8; AUX2L CHANNEL 1001: V9; AUX2R CHANNEL 1010: VA; AUX3L CHANNEL 1011: VB; AUX3R CHANNEL 1100: VC; AUX4L CHANNEL 1101: VD; AUX4R CHANNEL 1110: VE; AUX5 L CHANNEL 1111: VF; AUX5 R CHANNEL 0x10: V10; AUX6 L CHANNEL 0x11: V11; AUX6 R CHANNEL 0x12: V12; Main Sum CHANNEL

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
19:15	ASAFO4	R/W	0x03	OUTPUT SELECTION for DAFO4 $0 = MAIN/L CHANNEL $1 = MAIN/R CHANNEL $2 = SUB CHANNEL $3 = C CHANNEL $4 = SL CHANNEL $5 = SR CHANNEL $6 = AUX1L CHANNEL $7 = AUX1R CHANNEL $8 = AUX2L CHANNEL $9 = AUX2R CHANNEL $A = AUX3L CHANNEL $B = AUX3R CHANNEL $C = AUX4L CHANNEL $D = AUX4R CHANNEL $E = AUX5 L CHANNEL $F = AUX5 R CHANNEL $10 = AUX6 L CHANNEL $11 = AUX6 R CHANNEL $12 = Main Sum CHANNEL >$12 = reserved 0: V0; MAIN/L CHANNEL 1: V1; MAIN/R CHANNEL 10: V2; SUB CHANNEL 11: V3; C CHANNEL 100: V4; SL CHANNEL 101: V5; SR CHANNEL 110: V6; AUX1L CHANNEL 111: V7; AUX1R CHANNEL 1000: V8; AUX2L CHANNEL 1001: V9; AUX2R CHANNEL 1010: VA; AUX3L CHANNEL 1011: VB; AUX3R CHANNEL 1100: VC; AUX4L CHANNEL 1101: VD; AUX4R CHANNEL 1110: VE; AUX5 L CHANNEL 1111: VF; AUX5 R CHANNEL 0x10: V10; AUX6 L CHANNEL 0x11: V11; AUX6 R CHANNEL 0x12: V12; Main Sum CHANNEL
23:20	RSD_23To20	R/W	0x0	Not used, must be fixed to '0'

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
Offset 0x20	***ASW_AFO5_8_REG0***			
4:0	ASAFO5	R/W	0x04	OUTPUT SELECTION for DAFO5 $0 = MAIN/L CHANNEL $1 = MAIN/R CHANNEL $2 = SUB CHANNEL $3 = C CHANNEL $4 = SL CHANNEL $5 = SR CHANNEL $6 = AUX1L CHANNEL $7 = AUX1R CHANNEL $8 = AUX2L CHANNEL $9 = AUX2R CHANNEL $A = AUX3L CHANNEL $B = AUX3R CHANNEL $C = AUX4L CHANNEL $D = AUX4R CHANNEL $E = AUX5 L CHANNEL $F = AUX5 R CHANNEL $10 = AUX6 L CHANNEL $11 = AUX6 R CHANNEL $12 = Main Sum CHANNEL >$12 = reserved 0: V0; MAIN/L CHANNEL 1: V1; MAIN/R CHANNEL 10: V2; SUB CHANNEL 11: V3; C CHANNEL 100: V4; SL CHANNEL 101: V5; SR CHANNEL 110: V6; AUX1L CHANNEL 111: V7; AUX1R CHANNEL 1000: V8; AUX2L CHANNEL 1001: V9; AUX2R CHANNEL 1010: VA; AUX3L CHANNEL 1011: VB; AUX3R CHANNEL 1100: VC; AUX4L CHANNEL 1101: VD; AUX4R CHANNEL 1110: VE; AUX5 L CHANNEL 1111: VF; AUX5 R CHANNEL 0x10: V10; AUX6 L CHANNEL 0x11: V11; AUX6 R CHANNEL 0x12: V12; Main Sum CHANNEL

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
9:5	ASAFO6	R/W	0x05	OUTPUT SELECTION for DAFO6 $0 = MAIN/L CHANNEL $1 = MAIN/R CHANNEL $2 = SUB CHANNEL $3 = C CHANNEL $4 = SL CHANNEL $5 = SR CHANNEL $6 = AUX1L CHANNEL $7 = AUX1R CHANNEL $8 = AUX2L CHANNEL $9 = AUX2R CHANNEL $A = AUX3L CHANNEL $B = AUX3R CHANNEL $C = AUX4L CHANNEL $D = AUX4R CHANNEL $E = AUX5 L CHANNEL $F = AUX5 R CHANNEL $10 = AUX6 L CHANNEL $11 = AUX6 R CHANNEL $12 = Main Sum CHANNEL >$12 = reserved 0: V0; MAIN/L CHANNEL 1: V1; MAIN/R CHANNEL 10: V2; SUB CHANNEL 11: V3; C CHANNEL 100: V4; SL CHANNEL 101: V5; SR CHANNEL 110: V6; AUX1L CHANNEL 111: V7; AUX1R CHANNEL 1000: V8; AUX2L CHANNEL 1001: V9; AUX2R CHANNEL 1010: VA; AUX3L CHANNEL 1011: VB; AUX3R CHANNEL 1100: VC; AUX4L CHANNEL 1101: VD; AUX4R CHANNEL 1110: VE; AUX5 L CHANNEL 1111: VF; AUX5 R CHANNEL 0x10: V10; AUX6 L CHANNEL 0x11: V11; AUX6 R CHANNEL 0x12: V12; Main Sum CHANNEL

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
14:10	ASAFO7	R/W	0x06	OUTPUT SELECTION for DAFO7 $0 = MAIN/L CHANNEL $1 = MAIN/R CHANNEL $2 = SUB CHANNEL $3 = C CHANNEL $4 = SL CHANNEL $5 = SR CHANNEL $6 = AUX1L CHANNEL $7 = AUX1R CHANNEL $8 = AUX2L CHANNEL $9 = AUX2R CHANNEL $A = AUX3L CHANNEL $B = AUX3R CHANNEL $C = AUX4L CHANNEL $D = AUX4R CHANNEL $E = AUX5 L CHANNEL $F = AUX5 R CHANNEL $10 = AUX6 L CHANNEL $11 = AUX6 R CHANNEL $12 = Main Sum CHANNEL >$12 = reserved 0: V0; MAIN/L CHANNEL 1: V1; MAIN/R CHANNEL 10: V2; SUB CHANNEL 11: V3; C CHANNEL 100: V4; SL CHANNEL 101: V5; SR CHANNEL 110: V6; AUX1L CHANNEL 111: V7; AUX1R CHANNEL 1000: V8; AUX2L CHANNEL 1001: V9; AUX2R CHANNEL 1010: VA; AUX3L CHANNEL 1011: VB; AUX3R CHANNEL 1100: VC; AUX4L CHANNEL 1101: VD; AUX4R CHANNEL 1110: VE; AUX5 L CHANNEL 1111: VF; AUX5 R CHANNEL 0x10: V10; AUX6 L CHANNEL 0x11: V11; AUX6 R CHANNEL 0x12: V12; Main Sum CHANNEL

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
19:15	ASAFO8	R/W	0x07	OUTPUT SELECTION for DAFO8 $0 = MAIN/L CHANNEL $1 = MAIN/R CHANNEL $2 = SUB CHANNEL $3 = C CHANNEL $4 = SL CHANNEL $5 = SR CHANNEL $6 = AUX1L CHANNEL $7 = AUX1R CHANNEL $8 = AUX2L CHANNEL $9 = AUX2R CHANNEL $A = AUX3L CHANNEL $B = AUX3R CHANNEL $C = AUX4L CHANNEL $D = AUX4R CHANNEL $E = AUX5 L CHANNEL $F = AUX5 R CHANNEL $10 = AUX6 L CHANNEL $11 = AUX6 R CHANNEL $12 = Main Sum CHANNEL >$12 = reserved 0: V0; MAIN/L CHANNEL 1: V1; MAIN/R CHANNEL 10: V2; SUB CHANNEL 11: V3; C CHANNEL 100: V4; SL CHANNEL 101: V5; SR CHANNEL 110: V6; AUX1L CHANNEL 111: V7; AUX1R CHANNEL 1000: V8; AUX2L CHANNEL 1001: V9; AUX2R CHANNEL 1010: VA; AUX3L CHANNEL 1011: VB; AUX3R CHANNEL 1100: VC; AUX4L CHANNEL 1101: VD; AUX4R CHANNEL 1110: VE; AUX5 L CHANNEL 1111: VF; AUX5 R CHANNEL 0x10: V10; AUX6 L CHANNEL 0x11: V11; AUX6 R CHANNEL 0x12: V12; Main Sum CHANNEL
23:20	RSD_23To20	R/W	0x0	Not used, must be fixed to '0'

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
Offset 0x24	***ASW_DAC1_2_REG0***			
4:0	ASDAC1L	R/W	0x00	OUTPUT SELECTION for DAC1L $0 = MAIN/L CHANNEL $1 = MAIN/R CHANNEL $2 = SUB CHANNEL $3 = C CHANNEL $4 = SL CHANNEL $5 = SR CHANNEL $6 = AUX1L CHANNEL $7 = AUX1R CHANNEL $8 = AUX2L CHANNEL $9 = AUX2R CHANNEL $A = AUX3L CHANNEL $B = AUX3R CHANNEL $C = AUX4L CHANNEL $D = AUX4R CHANNEL $E = AUX5 L CHANNEL $F = AUX5 R CHANNEL $10 = AUX6 L CHANNEL $11 = AUX6 R CHANNEL $12 = Main Sum CHANNEL >$12 = reserved 0: V0; MAIN/L CHANNEL 1: V1; MAIN/R CHANNEL 10: V2; SUB CHANNEL 11: V3; C CHANNEL 100: V4; SL CHANNEL 101: V5; SR CHANNEL 110: V6; AUX1L CHANNEL 111: V7; AUX1R CHANNEL 1000: V8; AUX2L CHANNEL 1001: V9; AUX2R CHANNEL 1010: VA; AUX3L CHANNEL 1011: VB; AUX3R CHANNEL 1100: VC; AUX4L CHANNEL 1101: VD; AUX4R CHANNEL 1110: VE; AUX5 L CHANNEL 1111: VF; AUX5 R CHANNEL 0x10: V10; AUX6 L CHANNEL 0x11: V11; AUX6 R CHANNEL 0x12: V12; Main Sum CHANNEL

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
9:5	ASDAC1R	R/W	0x01	OUTPUT SELECTION for DAC1R $0 = MAIN/L CHANNEL $1 = MAIN/R CHANNEL $2 = SUB CHANNEL $3 = C CHANNEL $4 = SL CHANNEL $5 = SR CHANNEL $6 = AUX1L CHANNEL $7 = AUX1R CHANNEL $8 = AUX2L CHANNEL $9 = AUX2R CHANNEL $A = AUX3L CHANNEL $B = AUX3R CHANNEL $C = AUX4L CHANNEL $D = AUX4R CHANNEL $E = AUX5 L CHANNEL $F = AUX5 R CHANNEL $10 = AUX6 L CHANNEL $11 = AUX6 R CHANNEL $12 = Main Sum CHANNEL >$12 = reserved 0: V0; MAIN/L CHANNEL 1: V1; MAIN/R CHANNEL 10: V2; SUB CHANNEL 11: V3; C CHANNEL 100: V4; SL CHANNEL 101: V5; SR CHANNEL 110: V6; AUX1L CHANNEL 111: V7; AUX1R CHANNEL 1000: V8; AUX2L CHANNEL 1001: V9; AUX2R CHANNEL 1010: VA; AUX3L CHANNEL 1011: VB; AUX3R CHANNEL 1100: VC; AUX4L CHANNEL 1101: VD; AUX4R CHANNEL 1110: VE; AUX5 L CHANNEL 1111: VF; AUX5 R CHANNEL 0x10: V10; AUX6 L CHANNEL 0x11: V11; AUX6 R CHANNEL 0x12: V12; Main Sum CHANNEL

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
14:10	ASDAC2L	R/W	0x00	OUTPUT SELECTION for DAC2L $0 = MAIN/L CHANNEL $1 = MAIN/R CHANNEL $2 = SUB CHANNEL $3 = C CHANNEL $4 = SL CHANNEL $5 = SR CHANNEL $6 = AUX1L CHANNEL $7 = AUX1R CHANNEL $8 = AUX2L CHANNEL $9 = AUX2R CHANNEL $A = AUX3L CHANNEL $B = AUX3R CHANNEL $C = AUX4L CHANNEL $D = AUX4R CHANNEL $E = AUX5 L CHANNEL $F = AUX5 R CHANNEL $10 = AUX6 L CHANNEL $11 = AUX6 R CHANNEL $12 = Main Sum CHANNEL >$12 = reserved 0: V0; MAIN/L CHANNEL 1: V1; MAIN/R CHANNEL 10: V2; SUB CHANNEL 11: V3; C CHANNEL 100: V4; SL CHANNEL 101: V5; SR CHANNEL 110: V6; AUX1L CHANNEL 111: V7; AUX1R CHANNEL 1000: V8; AUX2L CHANNEL 1001: V9; AUX2R CHANNEL 1010: VA; AUX3L CHANNEL 1011: VB; AUX3R CHANNEL 1100: VC; AUX4L CHANNEL 1101: VD; AUX4R CHANNEL 1110: VE; AUX5 L CHANNEL 1111: VF; AUX5 R CHANNEL 0x10: V10; AUX6 L CHANNEL 0x11: V11; AUX6 R CHANNEL 0x12: V12; Main Sum CHANNEL

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
19:15	ASDAC2R	R/W	0x01	OUTPUT SELECTION for DAC2R $0 = MAIN/L CHANNEL $1 = MAIN/R CHANNEL $2 = SUB CHANNEL $3 = C CHANNEL $4 = SL CHANNEL $5 = SR CHANNEL $6 = AUX1L CHANNEL $7 = AUX1R CHANNEL $8 = AUX2L CHANNEL $9 = AUX2R CHANNEL $A = AUX3L CHANNEL $B = AUX3R CHANNEL $C = AUX4L CHANNEL $D = AUX4R CHANNEL $E = AUX5 L CHANNEL $F = AUX5 R CHANNEL $10 = AUX6 L CHANNEL $11 = AUX6 R CHANNEL $12 = Main Sum CHANNEL >$12 = reserved 0: V0; MAIN/L CHANNEL 1: V1; MAIN/R CHANNEL 10: V2; SUB CHANNEL 11: V3; C CHANNEL 100: V4; SL CHANNEL 101: V5; SR CHANNEL 110: V6; AUX1L CHANNEL 111: V7; AUX1R CHANNEL 1000: V8; AUX2L CHANNEL 1001: V9; AUX2R CHANNEL 1010: VA; AUX3L CHANNEL 1011: VB; AUX3R CHANNEL 1100: VC; AUX4L CHANNEL 1101: VD; AUX4R CHANNEL 1110: VE; AUX5 L CHANNEL 1111: VF; AUX5 R CHANNEL 0x10: V10; AUX6 L CHANNEL 0x11: V11; AUX6 R CHANNEL 0x12: V12; Main Sum CHANNEL
23:20	RSD_23To20	R/W	0x0	Not used, must be fixed to '0'

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
Offset 0x28	***ASW_I2S1_2_REG0***			
4:0	ASIIS1L	R/W	0x00	OUTPUT SELECTION for IIS1L $0 = MAIN/L CHANNEL $1 = MAIN/R CHANNEL $2 = SUB CHANNEL $3 = C CHANNEL $4 = SL CHANNEL $5 = SR CHANNEL $6 = AUX1L CHANNEL $7 = AUX1R CHANNEL $8 = AUX2L CHANNEL $9 = AUX2R CHANNEL $A = AUX3L CHANNEL $B = AUX3R CHANNEL $C = AUX4L CHANNEL $D = AUX4R CHANNEL $E = AUX5 L CHANNEL $F = AUX5 R CHANNEL $10 = AUX6 L CHANNEL $11 = AUX6 R CHANNEL $12 = Main Sum CHANNEL >$12 = reserved 0: V0; MAIN/L CHANNEL 1: V1; MAIN/R CHANNEL 10: V2; SUB CHANNEL 11: V3; C CHANNEL 100: V4; SL CHANNEL 101: V5; SR CHANNEL 110: V6; AUX1L CHANNEL 111: V7; AUX1R CHANNEL 1000: V8; AUX2L CHANNEL 1001: V9; AUX2R CHANNEL 1010: VA; AUX3L CHANNEL 1011: VB; AUX3R CHANNEL 1100: VC; AUX4L CHANNEL 1101: VD; AUX4R CHANNEL 1110: VE; AUX5 L CHANNEL 1111: VF; AUX5 R CHANNEL 0x10: V10; AUX6 L CHANNEL 0x11: V11; AUX6 R CHANNEL 0x12: V12; Main Sum CHANNEL

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
9:5	ASIIS1R	R/W	0x01	OUTPUT SELECTION for IIS1R $0 = MAIN/L CHANNEL $1 = MAIN/R CHANNEL $2 = SUB CHANNEL $3 = C CHANNEL $4 = SL CHANNEL $5 = SR CHANNEL $6 = AUX1L CHANNEL $7 = AUX1R CHANNEL $8 = AUX2L CHANNEL $9 = AUX2R CHANNEL $A = AUX3L CHANNEL $B = AUX3R CHANNEL $C = AUX4L CHANNEL $D = AUX4R CHANNEL $E = AUX5 L CHANNEL $F = AUX5 R CHANNEL $10 = AUX6 L CHANNEL $11 = AUX6 R CHANNEL $12 = Main Sum CHANNEL >$12 = reserved 0: V0; MAIN/L CHANNEL 1: V1; MAIN/R CHANNEL 10: V2; SUB CHANNEL 11: V3; C CHANNEL 100: V4; SL CHANNEL 101: V5; SR CHANNEL 110: V6; AUX1L CHANNEL 111: V7; AUX1R CHANNEL 1000: V8; AUX2L CHANNEL 1001: V9; AUX2R CHANNEL 1010: VA; AUX3L CHANNEL 1011: VB; AUX3R CHANNEL 1100: VC; AUX4L CHANNEL 1101: VD; AUX4R CHANNEL 1110: VE; AUX5 L CHANNEL 1111: VF; AUX5 R CHANNEL 0x10: V10; AUX6 L CHANNEL 0x11: V11; AUX6 R CHANNEL 0x12: V12; Main Sum CHANNEL

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
14:10	ASIIS2L	R/W	0x00	OUTPUT SELECTION for IIS2L $0 = MAIN/L CHANNEL $1 = MAIN/R CHANNEL $2 = SUB CHANNEL $3 = C CHANNEL $4 = SL CHANNEL $5 = SR CHANNEL $6 = AUX1L CHANNEL $7 = AUX1R CHANNEL $8 = AUX2L CHANNEL $9 = AUX2R CHANNEL $A = AUX3L CHANNEL $B = AUX3R CHANNEL $C = AUX4L CHANNEL $D = AUX4R CHANNEL $E = AUX5 L CHANNEL $F = AUX5 R CHANNEL $10 = AUX6 L CHANNEL $11 = AUX6 R CHANNEL $12 = Main Sum CHANNEL >$12 = reserved 0: V0; MAIN/L CHANNEL 1: V1; MAIN/R CHANNEL 10: V2; SUB CHANNEL 11: V3; C CHANNEL 100: V4; SL CHANNEL 101: V5; SR CHANNEL 110: V6; AUX1L CHANNEL 111: V7; AUX1R CHANNEL 1000: V8; AUX2L CHANNEL 1001: V9; AUX2R CHANNEL 1010: VA; AUX3L CHANNEL 1011: VB; AUX3R CHANNEL 1100: VC; AUX4L CHANNEL 1101: VD; AUX4R CHANNEL 1110: VE; AUX5 L CHANNEL 1111: VF; AUX5 R CHANNEL 0x10: V10; AUX6 L CHANNEL 0x11: V11; AUX6 R CHANNEL 0x12: V12; Main Sum CHANNEL

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
19:15	ASIIS2R	R/W	0x01	OUTPUT SELECTION for IIS2R $0 = MAIN/L CHANNEL $1 = MAIN/R CHANNEL $2 = SUB CHANNEL $3 = C CHANNEL $4 = SL CHANNEL $5 = SR CHANNEL $6 = AUX1L CHANNEL $7 = AUX1R CHANNEL $8 = AUX2L CHANNEL $9 = AUX2R CHANNEL $A = AUX3L CHANNEL $B = AUX3R CHANNEL $C = AUX4L CHANNEL $D = AUX4R CHANNEL $E = AUX5 L CHANNEL $F = AUX5 R CHANNEL $10 = AUX6 L CHANNEL $11 = AUX6 R CHANNEL $12 = Main Sum CHANNEL >$12 = reserved 0: V0; MAIN/L CHANNEL 1: V1; MAIN/R CHANNEL 10: V2; SUB CHANNEL 11: V3; C CHANNEL 100: V4; SL CHANNEL 101: V5; SR CHANNEL 110: V6; AUX1L CHANNEL 111: V7; AUX1R CHANNEL 1000: V8; AUX2L CHANNEL 1001: V9; AUX2R CHANNEL 1010: VA; AUX3L CHANNEL 1011: VB; AUX3R CHANNEL 1100: VC; AUX4L CHANNEL 1101: VD; AUX4R CHANNEL 1110: VE; AUX5 L CHANNEL 1111: VF; AUX5 R CHANNEL 0x10: V10; AUX6 L CHANNEL 0x11: V11; AUX6 R CHANNEL 0x12: V12; Main Sum CHANNEL
23:20	RSD_23To20	R/W	0x0	Not used, must be fixed to '0'

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
Offset 0x2C	***ASW_I2S3_4_REG0***			
4:0	ASIIS3L	R/W	0x00	OUTPUT SELECTION for IIS3L $0 = MAIN/L CHANNEL $1 = MAIN/R CHANNEL $2 = SUB CHANNEL $3 = C CHANNEL $4 = SL CHANNEL $5 = SR CHANNEL $6 = AUX1L CHANNEL $7 = AUX1R CHANNEL $8 = AUX2L CHANNEL $9 = AUX2R CHANNEL $A = AUX3L CHANNEL $B = AUX3R CHANNEL $C = AUX4L CHANNEL $D = AUX4R CHANNEL $E = AUX5 L CHANNEL $F = AUX5 R CHANNEL $10 = AUX6 L CHANNEL $11 = AUX6 R CHANNEL $12 = Main Sum CHANNEL >$12 = reserved 0: V0; MAIN/L CHANNEL 1: V1; MAIN/R CHANNEL 10: V2; SUB CHANNEL 11: V3; C CHANNEL 100: V4; SL CHANNEL 101: V5; SR CHANNEL 110: V6; AUX1L CHANNEL 111: V7; AUX1R CHANNEL 1000: V8; AUX2L CHANNEL 1001: V9; AUX2R CHANNEL 1010: VA; AUX3L CHANNEL 1011: VB; AUX3R CHANNEL 1100: VC; AUX4L CHANNEL 1101: VD; AUX4R CHANNEL 1110: VE; AUX5 L CHANNEL 1111: VF; AUX5 R CHANNEL 0x10: V10; AUX6 L CHANNEL 0x11: V11; AUX6 R CHANNEL 0x12: V12; Main Sum CHANNEL

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
9:5	ASIIS3R	R/W	0x01	OUTPUT SELECTION for IIS3R $0 = MAIN/L CHANNEL $1 = MAIN/R CHANNEL $2 = SUB CHANNEL $3 = C CHANNEL $4 = SL CHANNEL $5 = SR CHANNEL $6 = AUX1L CHANNEL $7 = AUX1R CHANNEL $8 = AUX2L CHANNEL $9 = AUX2R CHANNEL $A = AUX3L CHANNEL $B = AUX3R CHANNEL $C = AUX4L CHANNEL $D = AUX4R CHANNEL $E = AUX5 L CHANNEL $F = AUX5 R CHANNEL $10 = AUX6 L CHANNEL $11 = AUX6 R CHANNEL $12 = Main Sum CHANNEL >$12 = reserved 0: V0; MAIN/L CHANNEL 1: V1; MAIN/R CHANNEL 10: V2; SUB CHANNEL 11: V3; C CHANNEL 100: V4; SL CHANNEL 101: V5; SR CHANNEL 110: V6; AUX1L CHANNEL 111: V7; AUX1R CHANNEL 1000: V8; AUX2L CHANNEL 1001: V9; AUX2R CHANNEL 1010: VA; AUX3L CHANNEL 1011: VB; AUX3R CHANNEL 1100: VC; AUX4L CHANNEL 1101: VD; AUX4R CHANNEL 1110: VE; AUX5 L CHANNEL 1111: VF; AUX5 R CHANNEL 0x10: V10; AUX6 L CHANNEL 0x11: V11; AUX6 R CHANNEL 0x12: V12; Main Sum CHANNEL

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
14:10	ASIIS4L	R/W	0x00	OUTPUT SELECTION for IIS4L $0 = MAIN/L CHANNEL $1 = MAIN/R CHANNEL $2 = SUB CHANNEL $3 = C CHANNEL $4 = SL CHANNEL $5 = SR CHANNEL $6 = AUX1L CHANNEL $7 = AUX1R CHANNEL $8 = AUX2L CHANNEL $9 = AUX2R CHANNEL $A = AUX3L CHANNEL $B = AUX3R CHANNEL $C = AUX4L CHANNEL $D = AUX4R CHANNEL $E = AUX5 L CHANNEL $F = AUX5 R CHANNEL $10 = AUX6 L CHANNEL $11 = AUX6 R CHANNEL $12 = Main Sum CHANNEL >$12 = reserved 0: V0; MAIN/L CHANNEL 1: V1; MAIN/R CHANNEL 10: V2; SUB CHANNEL 11: V3; C CHANNEL 100: V4; SL CHANNEL 101: V5; SR CHANNEL 110: V6; AUX1L CHANNEL 111: V7; AUX1R CHANNEL 1000: V8; AUX2L CHANNEL 1001: V9; AUX2R CHANNEL 1010: VA; AUX3L CHANNEL 1011: VB; AUX3R CHANNEL 1100: VC; AUX4L CHANNEL 1101: VD; AUX4R CHANNEL 1110: VE; AUX5 L CHANNEL 1111: VF; AUX5 R CHANNEL 0x10: V10; AUX6 L CHANNEL 0x11: V11; AUX6 R CHANNEL 0x12: V12; Main Sum CHANNEL

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
19:15	ASIIS4R	R/W	0x01	OUTPUT SELECTION for IIS4R $0 = MAIN/L CHANNEL $1 = MAIN/R CHANNEL $2 = SUB CHANNEL $3 = C CHANNEL $4 = SL CHANNEL $5 = SR CHANNEL $6 = AUX1L CHANNEL $7 = AUX1R CHANNEL $8 = AUX2L CHANNEL $9 = AUX2R CHANNEL $A = AUX3L CHANNEL $B = AUX3R CHANNEL $C = AUX4L CHANNEL $D = AUX4R CHANNEL $E = AUX5 L CHANNEL $F = AUX5 R CHANNEL $10 = AUX6 L CHANNEL $11 = AUX6 R CHANNEL $12 = Main Sum CHANNEL >$12 = reserved 0: V0; MAIN/L CHANNEL 1: V1; MAIN/R CHANNEL 10: V2; SUB CHANNEL 11: V3; C CHANNEL 100: V4; SL CHANNEL 101: V5; SR CHANNEL 110: V6; AUX1L CHANNEL 111: V7; AUX1R CHANNEL 1000: V8; AUX2L CHANNEL 1001: V9; AUX2R CHANNEL 1010: VA; AUX3L CHANNEL 1011: VB; AUX3R CHANNEL 1100: VC; AUX4L CHANNEL 1101: VD; AUX4R CHANNEL 1110: VE; AUX5 L CHANNEL 1111: VF; AUX5 R CHANNEL 0x10: V10; AUX6 L CHANNEL 0x11: V11; AUX6 R CHANNEL 0x12: V12; Main Sum CHANNEL
23:20	RSD_23To20	R/W	0x0	Not used, must be fixed to '0'

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
Offset 0x30	***ASW_I2S5_6_REG0***			
4:0	ASIIS5L	R/W	0x00	OUTPUT SELECTION for IIS5L $0 = MAIN/L CHANNEL $1 = MAIN/R CHANNEL $2 = SUB CHANNEL $3 = C CHANNEL $4 = SL CHANNEL $5 = SR CHANNEL $6 = AUX1L CHANNEL $7 = AUX1R CHANNEL $8 = AUX2L CHANNEL $9 = AUX2R CHANNEL $A = AUX3L CHANNEL $B = AUX3R CHANNEL $C = AUX4L CHANNEL $D = AUX4R CHANNEL $E = AUX5 L CHANNEL $F = AUX5 R CHANNEL $10 = AUX6 L CHANNEL $11 = AUX6 R CHANNEL $12 = Main Sum CHANNEL >$12 = reserved 0: V0; MAIN/L CHANNEL 1: V1; MAIN/R CHANNEL 10: V2; SUB CHANNEL 11: V3; C CHANNEL 100: V4; SL CHANNEL 101: V5; SR CHANNEL 110: V6; AUX1L CHANNEL 111: V7; AUX1R CHANNEL 1000: V8; AUX2L CHANNEL 1001: V9; AUX2R CHANNEL 1010: VA; AUX3L CHANNEL 1011: VB; AUX3R CHANNEL 1100: VC; AUX4L CHANNEL 1101: VD; AUX4R CHANNEL 1110: VE; AUX5 L CHANNEL 1111: VF; AUX5 R CHANNEL 0x10: V10; AUX6 L CHANNEL 0x11: V11; AUX6 R CHANNEL 0x12: V12; Main Sum CHANNEL

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
9:5	ASIIS5R	R/W	0x01	OUTPUT SELECTION for IIS5R $0 = MAIN/L CHANNEL $1 = MAIN/R CHANNEL $2 = SUB CHANNEL $3 = C CHANNEL $4 = SL CHANNEL $5 = SR CHANNEL $6 = AUX1L CHANNEL $7 = AUX1R CHANNEL $8 = AUX2L CHANNEL $9 = AUX2R CHANNEL $A = AUX3L CHANNEL $B = AUX3R CHANNEL $C = AUX4L CHANNEL $D = AUX4R CHANNEL $E = AUX5 L CHANNEL $F = AUX5 R CHANNEL $10 = AUX6 L CHANNEL $11 = AUX6 R CHANNEL $12 = Main Sum CHANNEL >$12 = reserved 0: V0; MAIN/L CHANNEL 1: V1; MAIN/R CHANNEL 10: V2; SUB CHANNEL 11: V3; C CHANNEL 100: V4; SL CHANNEL 101: V5; SR CHANNEL 110: V6; AUX1L CHANNEL 111: V7; AUX1R CHANNEL 1000: V8; AUX2L CHANNEL 1001: V9; AUX2R CHANNEL 1010: VA; AUX3L CHANNEL 1011: VB; AUX3R CHANNEL 1100: VC; AUX4L CHANNEL 1101: VD; AUX4R CHANNEL 1110: VE; AUX5 L CHANNEL 1111: VF; AUX5 R CHANNEL 0x10: V10; AUX6 L CHANNEL 0x11: V11; AUX6 R CHANNEL 0x12: V12; Main Sum CHANNEL

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
14:10	ASIIS6L	R/W	0x00	OUTPUT SELECTION for IIS6L $0 = MAIN/L CHANNEL $1 = MAIN/R CHANNEL $2 = SUB CHANNEL $3 = C CHANNEL $4 = SL CHANNEL $5 = SR CHANNEL $6 = AUX1L CHANNEL $7 = AUX1R CHANNEL $8 = AUX2L CHANNEL $9 = AUX2R CHANNEL $A = AUX3L CHANNEL $B = AUX3R CHANNEL $C = AUX4L CHANNEL $D = AUX4R CHANNEL $E = AUX5 L CHANNEL $F = AUX5 R CHANNEL $10 = AUX6 L CHANNEL $11 = AUX6 R CHANNEL $12 = Main Sum CHANNEL >$12 = reserved 0: V0; MAIN/L CHANNEL 1: V1; MAIN/R CHANNEL 10: V2; SUB CHANNEL 11: V3; C CHANNEL 100: V4; SL CHANNEL 101: V5; SR CHANNEL 110: V6; AUX1L CHANNEL 111: V7; AUX1R CHANNEL 1000: V8; AUX2L CHANNEL 1001: V9; AUX2R CHANNEL 1010: VA; AUX3L CHANNEL 1011: VB; AUX3R CHANNEL 1100: VC; AUX4L CHANNEL 1101: VD; AUX4R CHANNEL 1110: VE; AUX5 L CHANNEL 1111: VF; AUX5 R CHANNEL 0x10: V10; AUX6 L CHANNEL 0x11: V11; AUX6 R CHANNEL 0x12: V12; Main Sum CHANNEL

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
19:15	ASIIS6R	R/W	0x01	OUTPUT SELECTION for IIS6R $0 = MAIN/L CHANNEL $1 = MAIN/R CHANNEL $2 = SUB CHANNEL $3 = C CHANNEL $4 = SL CHANNEL $5 = SR CHANNEL $6 = AUX1L CHANNEL $7 = AUX1R CHANNEL $8 = AUX2L CHANNEL $9 = AUX2R CHANNEL $A = AUX3L CHANNEL $B = AUX3R CHANNEL $C = AUX4L CHANNEL $D = AUX4R CHANNEL $E = AUX5 L CHANNEL $F = AUX5 R CHANNEL $10 = AUX6 L CHANNEL $11 = AUX6 R CHANNEL $12 = Main Sum CHANNEL >$12 = reserved 0: V0; MAIN/L CHANNEL 1: V1; MAIN/R CHANNEL 10: V2; SUB CHANNEL 11: V3; C CHANNEL 100: V4; SL CHANNEL 101: V5; SR CHANNEL 110: V6; AUX1L CHANNEL 111: V7; AUX1R CHANNEL 1000: V8; AUX2L CHANNEL 1001: V9; AUX2R CHANNEL 1010: VA; AUX3L CHANNEL 1011: VB; AUX3R CHANNEL 1100: VC; AUX4L CHANNEL 1101: VD; AUX4R CHANNEL 1110: VE; AUX5 L CHANNEL 1111: VF; AUX5 R CHANNEL 0x10: V10; AUX6 L CHANNEL 0x11: V11; AUX6 R CHANNEL 0x12: V12; Main Sum CHANNEL
23:20	RSD_23To20	R/W	0x0	Not used, must be fixed to '0'
Offset 0x34	***ASW_MUT_CON_REG0***			
0	MAINMUT	R/W	0x1	Softmute MAIN/L,R output 0: V0; OFF 1: V1; ON
1	MAINLMUT	R/W	0x0	Softmute MAIN/L output 0: V0; OFF 1: V1; ON
2	MAINRMUT	R/W	0x0	Softmute MAIN/R output 0: V0; OFF 1: V1; ON
3	SWMUT	R/W	0x1	Softmute SUBWOOFER output 0: V0; OFF 1: V1; ON

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
4	CMUT	R/W	0x1	Softmute CENTER output 0: V0; OFF 1: V1; ON
5	SLMUT	R/W	0x1	Softmute SURROUND Left output 0: V0; OFF 1: V1; ON
6	SRMUT	R/W	0x1	Softmute SURROUND Right output 0: V0; OFF 1: V1; ON
7	AUX1MUT	R/W	0x1	Softmute AUX1 outputs 0: V0; OFF 1: V1; ON
8	AUX2MUT	R/W	0x1	Mute AUX2 outputs 0: V0; OFF 1: V1; ON
9	AUX3MUT	R/W	0x1	Mute AUX3 outputs 0: V0; OFF 1: V1; ON
10	AUX4MUT	R/W	0x1	Mute AUX4 outputs 0: V0; OFF 1: V1; ON
11	AUX5MUT	R/W	0x1	Mute AUX5 outputs 0: V0; OFF 1: V1; ON
12	AUX6MUT	R/W	0x1	Softmute AUX6 output 0: V0; OFF 1: V1; ON
23:13	RSD_23To13	R/W	0x000	Not used, must be fixed to '0'
Offset 0x38	***LEV_ADJ_ADC_DEMDEC_IIS_REG0***			
4:0	DECLEV	R/W	0x00	Level adjust DEC (+15..-15dB)(-16 = MUTE) 15 = +15 dB .. -16 = MUTE 1111: V15; +15 dB 0x10: Minus_16; MUTE
9:5	MONOLEV	R/W	0x00	Level adjust MONO (+15..-15dB)(-16 = MUTE) 15 = +15 dB .. -16 = MUTE 1111: V15; +15 dB 0x10: Minus_16; MUTE
14:10	SAPLEV	R/W	0x00	Level adjust SAP (+15..-15dB)(-16 = MUTE) 15 = +15 dB .. -16 = MUTE 1111: V15; +15 dB 0x10: Minus_16; MUTE

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
19:15	PIPMONOLEV	R/W	0x00	Level adjust PIPMONO (+15..-15dB)(-16 = MUTE) 15 = +15 dB .. -16 = MUTE 1111: V15; +15 dB 0x10: Minus_16; MUTE
23:20	RSD_23To20	R/W	0x0	Not used, must be fixed to '0'
Offset 0x3C	***LEV_ADJ_ADC_IIS_REG0***			
4:0	ADCL_ALEV	R/W	0x00	Level adjust ADC L/A INPUT (+15..-15dB)(-16 = MUTE) 15 = +15 dB .. -16 = MUTE 1111: V15; +15 dB 0x10: Minus_16; MUTE
9:5	ADCR_BLEV	R/W	0x00	Level adjust ADC R/B INPUT (+15..-15dB)(-16 = MUTE) 15 = +15 dB .. -16 = MUTE 1111: V15; +15 dB 0x10: Minus_16; MUTE
14:10	IIS1LEV	R/W	0x00	Level adjust IIS1 INPUT (+15..-15dB)(-16 = MUTE) 15 = +15 dB .. -16 = MUTE 1111: V15; +15 dB 0x10: Minus_16; MUTE
19:15	IIS2LEV	R/W	0x00	Level adjust IIS2 INPUT (+15..-15dB)(-16 = MUTE) 15 = +15 dB .. -16 = MUTE 1111: V15; +15 dB 0x10: Minus_16; MUTE
23:20	RSD_23To20	R/W	0x0	Not used, must be fixed to '0'
Offset 0x40	***LEV_ADJ_IIS3_4_5_6_REG0***			
4:0	IIS3LEV	R/W	0x00	Level adjust IIS3 INPUT (+15..-15dB)(-16 = MUTE) 15 = +15 dB .. -16 = MUTE 1111: V15; +15 dB 0x10: Minus_16; MUTE
9:5	IIS4LEV	R/W	0x00	Level adjust IIS4 INPUT (+15..-15dB)(-16 = MUTE) 15 = +15 dB .. -16 = MUTE 1111: V15; +15 dB 0x10: Minus_16; MUTE
14:10	IIS5LEV	R/W	0x00	Level adjust IIS5 INPUT (+15..-15dB)(-16 = MUTE) 15 = +15 dB .. -16 = MUTE 1111: V15; +15 dB 0x10: Minus_16; MUTE
19:15	IIS6LEV	R/W	0x00	Level adjust IIS6 INPUT (+15..-15dB)(-16 = MUTE) 15 = +15 dB .. -16 = MUTE 1111: V15; +15 dB 0x10: Minus_16; MUTE
23:20	RSD_23To20	R/W	0x0	Not used, must be fixed to '0'
Offset 0x44	***SOU_APP_MOD_REG0***			
0	EXEMODTAB	R/W	0x0	Execute 'Mode Table'

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
5:1	SNDMOD	R/W	0x00	Sound Modes 0: V0; Mono/Stereo (default) 1: V1; Mono/Stereo (Hall) 10: V2; Mono/Stereo (Matrix) 11: V3; DPLII (Wide Center) 100: V4; DPLII (3 Stereo) 101: V5; DPLII (Phantom Center) 110: V6; VDS 522 111: V7; VDS 523 1000: V8; VDD 522 1001: V9; VDD 523 1010: VA; Noise Sequencing 1011: VB; Active Surround
8:6	CLIPMANAGE	R/W	0x0	Clip Management 0: V0; Clip management OFF (default) 1: V1; Static Volume Mode 10: V2; Static Control Mode 11: V3; Dynamic Control Mode 100: V4; Dynamic Volume Mode 101: V5; Reserved 110: V6; Reserved 111: V7; Reserved
12:9	DVMLEV	R/W	0x0	Dynamic Volume Mode, none attack level 0: V0; -3dB 1: V1; -4dB 10: V2; -5dB 11: V3; -6dB 100: V4; -7dB 101: V5; -8dB 110: V6; -9dB 111: V7; -10dB 1000: V8; -11dB 1001: V9; -12dB 1010: VA; -13dB 1011: VB; -14dB 1100: VC; -15dB 1101: VD; -16dB 1110: VE; -17dB 1111: VF; -18dB
13	CENTERMUTE	R/W	0x0	Hall, Matrix Center Mute 0: V0; Center channel ON (default) 1: V1; Center channel OFF
23:14	RSD_23To14	R/W	0x000	Not used, must be fixed to '0'

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
Offset 0x48	***SOU_EFF_REG0***			
1:0	INSOMO	R/W	0x0	Incredible sound mode 0: V0; OFF 1: V1; ISTEREO 10: V2; IMONO
4:2	INSOEF	R/W	0x0	Incredible Mono/Stereo Effect: 0..100% (5 steps) 0: V0; 0% 1: V1; 20% 10: V2; 40% 11: V3; 60% 100: V4; 80% 101: V5; 100%
7:5	AVLMOD	R/W	0x0	AVL mode 0: V0; OFF/reset 1: V1; very short decay (20msec) 10: V2; extra short decay (2sec) 11: V3; short decay (4sec) 100: V4; medium decay (8sec) 101: V5; long decay (16sec)
8	AVLWEIGHT	R/W	0x0	AVL weighting filter 0: V0; OFF 1: V1; ON
12:9	AVLLEV	R/W	0x0	AVL reference level (16 steps: -6,-8,... -36 dBFS) $x = to be fixed (living room) $y = to be fixed (sleeping room) 0: Vx; to be fixed (living room)
23:13	RSD_23To13	R/W	0x000	Not used, must be fixed to '0'
Offset 0x4C	***SOU_BASS_EFF_REG0***			
3:0	BBECONTOUR	R/W	0x0	BBE Contour value 0: V0; Min. bass boost 1: V1; Max. bass boost
7:4	BBEPROCESS	R/W	0x0	BBE Process value 0: V0; Min. process 1: V1; Max. process
9:8	BBELOUDCTRL	R/W	0x0	Loudness and BBE control 0: V0; Loudness and BBE OFF 1: V1; Loudness ON 10: V2; BBE ON

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
12:10	MAINLONA	R/W	0x0	MAIN loudness none attack volume level 0: V0; -15dB Volume 1: V1; -12dB Volume 10: V2; -9dB Volume 11: V3; -6dB Volume 100: V4; -3dB Volume 101: V5; 0dB Volume 110: V6; +3dB Volume 111: V7; +6dB Volume
14:13	MAINLOCH	R/W	0x0	MAIN loudness filter characteristic (bass/treble in dB) $0 = standard (500Hz) $1 = extra bass (1000Hz) bass: 20 Hz -> max. 18.3 dB treble: 16 kHz -> max. 4.3 dB 0: V0; standard (500Hz) 1: V1; extra bass (1000Hz)
17:15	DBEDUBCTRL	R/W	0x0	DBE and DUB control 0: V0; DBE and DUB Off 1: V1; DBE main channel On 10: V2; DUB main channel On 11: V3; DBE subwoofer channel On 100: V4; DUB subwoofer channel On
23:18	RSD_23To18	R/W	0x00	Not used, must be fixed to '0'
Offset 0x50	***DBE_COEF_DOWNL_REG0***			
5:0	DBEADR	R/W	0x00	DBE coefficient address
11:6	RSD_11To6	R/W	0x00	Reserved
23:12	DBECOEF	R/W	0x000	DBE coefficients
Offset 0x54	***DUB_COEF_DOWNL_REG0***			
7:0	DUBADR	R/W	0x00	DUB coefficient address
11:8	RSD_11To8	R/W	0x0	Reserved
23:12	DUBCOEF	R/W	0x000	DUB coefficients
Offset 0x58	***DOL_CON_REG0***			
2:0	VDDMIXLEV	R/W	0x0	VDD Mix Level mix level: 0..100% (5 steps) $0 = 0% (Minimum effect) $1 = 20% $2 = 40% $3 = 60% $4 = 80% $5 = 100% (Maximum effect) >$5 = reserved 0: V0; 0% (Minimum effect) 1: V1; 20% 10: V2; 40% 11: V3; 60% 100: V4; 80% 101: V5; 100% (Maximum effect)

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
5:3	BAMAMO	R/W	0x0	Bass management mode 0: V0; OFF (Wide Centre Mode) 1: V1; TYP1 configuration (Normal Centre Mode) 10: V2; TYP2 configuration (Normal Centre Mode) 11: V3; TYP3 configuration (Normal Centre Mode) 100: V4; TYP4 configuration (Normal Centre Mode)
6	BAMASUB	R/W	0x0	Bass Management subwoofer filter control 0: V0; Subwoofer filter Off 1: V1; Subwoofer filter On
10:7	BAMAFC	R/W	0x0	Bass management lowpass filtercharacteristics: 50 - 400Hz (in 4 Bit resolution)) cornerfrequency. Highpass filter is 1/ lowpass. 0: V0; 50 Hz 1: V1; 60 Hz 10: V2; 70 Hz 11: V3; 80 Hz 100: V4; 90 Hz 101: V5; 100 Hz 110: V6; 110 Hz 111: V7; 120 Hz 1000: V8; 130 Hz 1001: V9; 140 Hz 1010: VA; 150 Hz 1011: VB; 200 Hz 1100: VC; 250 Hz 1101: VD; 300 Hz 1110: VE; 350 Hz 1111: VF; 400 Hz

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
15:11	DPLDEL	R/W	0x00	Delayline values: Mono 1..62 ms in 31 steps. Stereo: 1..31 ms in 31 steps (Mono/Stereo). 0: V00; No delay 1: V01; 2ms / 1ms 10: V02; 4ms / 2ms 11: V03; 6ms / 3ms 100: V04; 8ms / 4ms 101: V05; 10ms / 5ms 110: V06; 12ms / 6ms 111: V07; 14ms / 7ms 1000: V08; 16ms / 8ms 1001: V09; 18ms / 9ms 1010: V0A; 20ms / 10ms 1011: V0B; 22ms / 11ms 1100: V0C; 24ms / 12ms 1101: V0D; 26ms / 13ms 1110: V0E; 28ms / 14ms 1111: V0F; 30ms / 15ms 0x10: V10; 32ms / 16ms 0x11: V11; 34ms / 17ms 0x12: V12; 36ms / 18ms 0x13: V13; 38ms / 19ms 0x14: V14; 40ms / 20ms 0x15: V15; 42ms / 21ms 0x16: V16; 44ms / 22ms 0x17: V17; 46ms / 23ms 0x18: V18; 48ms / 24ms 0x19: V19; 50ms / 25ms 0x1A: V1A; 52ms / 26ms 0x1B: V1B; 54ms / 27ms 0x1C: V1C; 56ms / 28ms 0x1D: V1D; 58ms / 29ms 0x1E: V1E; 60ms / 30ms 0x1F: V1F; 62ms / 31ms
18:16	DPL2MODE	R/W	0x0	Dolby Prologic II Modes 0: V0; Movie Mode 1: V1; Matrix Mode 10: V2; Music Mode 11: V3; Pro Logic Mode 100: V4; Virtual Mode

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
21:19	CENTERDEL	R/W	0x0	Delay values for the center channel signal in Dolby Digital mode: 0: V00; No delay 1: V01; 1ms 10: V02; 2ms 11: V03; 3ms 100: V04; 4ms 101: V05; 5ms 110: V06; 6ms 111: V07; 7ms
23:22	RSD_23To22	R/W	0x0	Not used, must be fixed to '0'
Offset 0x5C	***MAS_BEE_CON_REG0***			
10:0	MASTVOL	R/W	0x000	MASTER volume: (+24..-83.875dB, mute), controls MAIN, SW, C and S in 1/8dB steps 192 = +24.000 dB 191 = +23.875 dB .. 184 = +23.000 dB .. 0 = 0.000 dB -1 = -0.125 dB .. -671 = -83.875 dB -672 = mute 0: V0; 0.000 dB 0xB8: V184; +23.000 dB 0xBF: V191; +23.875 dB 0xC0: V192; +24.000 dB 0x560: Minus_672; mute 0x561: Minus_671; -83.875 dB 0x7FF: Minus_1; -0.125 dB
18:11	BEEPVOL	R/W	0xAC	BEEPER volume: (0..-83dB, mute) 0 = 0 dB -1 = -1 dB .. -84 = mute 0: V0; 0 dB 0xAC: Minus_84; mute 0xFF: Minus_1; -1 dB
21:19	BEEPFRE	R/W	0x0	BEEPER frequency:200..12500 Hz 0: V0; 200 Hz 1: V1; 400 Hz 10: V2; 1000 Hz 11: V3; 2000 Hz 100: V4; 3000 Hz 101: V5; 5000 Hz 110: V6; 8000 Hz 111: V7; 12500 Hz
23:22	RSD_23To22	R/W	0x0	Not used, must be fixed to '0'
Offset 0x60	***MAI_VOL_REG0***			
7:0	MAINVOLL	R/W	0x00	MAIN volume left: (+24..-83dB, mute) 24 = +24 dB 23 = +23 dB .. -84 = mute 0x17: V23; +23 dB 0x18: V24; +24 dB 0xAC: Minus_84; mute

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
15:8	MAINVOLR	R/W	0x00	MAIN volume right: (+24..-83dB, mute) 24 = +24 dB 23 = +23 dB .. -84 = mute 0x17: V23; +23 dB 0x18: V24; +24 dB 0xAC: Minus_84; mute
23:16	RSD_23To16	R/W	0x00	Not used, must be fixed to '0'
Offset 0x64	***SW_C_VOL_REG0***			
7:0	SWVOL	R/W	0x00	SUBWOOFER volume: (+24..-83dB, mute) 24 = +24 dB 23 = +23 dB .. -84 = mute 0x17: V23; +23 dB 0x18: V24; +24 dB 0xAC: Minus_84; mute
15:8	CVOL	R/W	0x00	CENTER volume: (+24..-83dB, mute) 24 = +24 dB 23 = +23 dB .. -84 = mute 0x17: V23; +23 dB 0x18: V24; +24 dB 0xAC: Minus_84; mute
23:16	RSD_23To16	R/W	0x00	Not used, must be fixed to '0'
Offset 0x68	***LS_RS_VOL_REG0***			
7:0	SLVOL	R/W	0x00	SURROUND volume left: (+24..-83dB, mute) 24 = +24 dB 23 = +23 dB .. -84 = mute 0x17: V23; +23 dB 0x18: V24; +24 dB 0xAC: Minus_84; mute
15:8	SRVOL	R/W	0x00	SURROUND volume right: (+24..-83dB, mute) 24 = +24 dB 23 = +23 dB .. -84 = mute 0x17: V23; +23 dB 0x18: V24; +24 dB 0xAC: Minus_84; mute
23:16	RSD_23To16	R/W	0x00	Not used, must be fixed to '0'
Offset 0x6C	***A1_VOL_REG0***			
7:0	AUX1VOLL	R/W	0x00	AUX1 volume left: (+24..-83dB, mute) 24 = +24 dB 23 = +23 dB .. -84 = mute 0x17: V23; +23 dB 0x18: V24; +24 dB 0xAC: Minus_84; mute
15:8	AUX1VOLR	R/W	0x00	AUX1 volume right: (+24..-83dB, mute) 24 = +24 dB 23 = +23 dB .. -84 = mute 0x17: V23; +23 dB 0x18: V24; +24 dB 0xAC: Minus_84; mute
23:16	RSD_23To16	R/W	0x00	Not used, must be fixed to '0'

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
Offset 0x70	***A2_VOL_REG0***			
7:0	AUX2VOLL	R/W	0x00	AUX2 volume left: (+24..-83dB, mute) 24 = +24 dB 23 = +23 dB .. -84 = mute 0x17: V23; +23 dB 0x18: V24; +24 dB 0xAC: Minus_84; mute
15:8	AUX2VOLR	R/W	0x00	AUX2 volume right: (+24..-83dB, mute) 24 = +24 dB 23 = +23 dB .. -84 = mute 0x17: V23; +23 dB 0x18: V24; +24 dB 0xAC: Minus_84; mute
23:16	RSD_23To16	R/W	0x00	Not used, must be fixed to '0'
Offset 0x74	***A3_VOL_REG0***			
7:0	AUX3VOLL	R/W	0x00	AUX3 volume left: (+24..-83dB, mute) 24 = +24 dB 23 = +23 dB .. -84 = mute 0x17: V23; +23 dB 0x18: V24; +24 dB 0xAC: Minus_84; mute
15:8	AUX3VOLR	R/W	0x00	AUX3 volume right: (+24..-83dB, mute) 24 = +24 dB 23 = +23 dB .. -84 = mute 0x17: V23; +23 dB 0x18: V24; +24 dB 0xAC: Minus_84; mute
23:16	RSD_23To16	R/W	0x00	Not used, must be fixed to '0'
Offset 0x78	***A4_VOL_REG0***			
7:0	AUX4VOLL	R/W	0x00	AUX4 volume left: (+24..-83dB, mute) 24 = +24 dB 23 = +23 dB .. -84 = mute 0x17: V23; +23 dB 0x18: V24; +24 dB 0xAC: Minus_84; mute
15:8	AUX4VOLR	R/W	0x00	AUX4 volume right: (+24..-83dB, mute) 24 = +24 dB 23 = +23 dB .. -84 = mute 0x17: V23; +23 dB 0x18: V24; +24 dB 0xAC: Minus_84; mute
23:16	RSD_23To16	R/W	0x00	Not used, must be fixed to '0'
Offset 0x7C	***A5_VOL_REG0***			
7:0	AUX5VOLL	R/W	0x00	AUX5 volume left: (+24..-83dB, mute) 24 = +24 dB 23 = +23 dB .. -84 = mute 0x17: V23; +23 dB 0x18: V24; +24 dB 0xAC: Minus_84; mute

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
15:8	AUX5VOLR	R/W	0x00	AUX5 volume right: (+24..-83dB, mute) 24 = +24 dB 23 = +23 dB .. -84 = mute 0x17: V23; +23 dB 0x18: V24; +24 dB 0xAC: Minus_84; mute
23:16	RSD_23To16	R/W	0x00	Not used, must be fixed to '0'
Offset 0x80	***A6_VOL_REG0***			
7:0	AUX6VOLL	R/W	0x00	AUX6 volume left: (+24..-83dB, mute) 24 = +24 dB 23 = +23 dB .. -84 = mute 0x17: V23; +23 dB 0x18: V24; +24 dB 0xAC: Minus_84; mute
15:8	AUX6VOLR	R/W	0x00	AUX6 volume right: (+24..-83dB, mute) 24 = +24 dB 23 = +23 dB .. -84 = mute 0x17: V23; +23 dB 0x18: V24; +24 dB 0xAC: Minus_84; mute
23:16	RSD_23To16	R/W	0x00	Not used, must be fixed to '0'
Offset 0x84	***MAI_TON_CON_REG0***			
4:0	MAINBASS	R/W	0x00	MAIN bass: (+15..-16dB, 1 dB steps) 15 = +15 dB .. -16 = -16 dB 1111: V15; +15 dB 0x10: Minus_16; -16 dB
9:5	MAINTREB	R/W	0x00	MAIN treble: (+15..-16dB, 1 dB steps) 15 = +15 dB .. -16 = -16 dB 1111: V15; +15 dB 0x10: Minus_16; -16 dB
12:10	MAINSMSO	R/W	0x0	MAIN smartsound: Predefined bass/treble settings
23:13	RSD_23To13	R/W	0x000	Not used, must be fixed to '0'
Offset 0x88	***CENTER_LFE_TON_CON_REG0***			
4:0	CENTERBASS	R/W	0x00	CENTER bass: (+15..-16dB, 1 dB steps) 15 = +15 dB .. -16 = -16 dB 1111: V15; +15 dB 0x10: Minus_16; -16 dB
9:5	CENTERTREB	R/W	0x00	CENTER treble: (+15..-16dB, 1 dB steps) 15 = +15 dB .. -16 = -16 dB 1111: V15; +15 dB 0x10: Minus_16; -16 dB
14:10	LFELEVEL	R/W	0x00	LFE Level: (+15..-15dB, 1 dB steps) 15 = +15 dB .. -15 = -15dB -16 = Mute 1111: V15; +15 dB 0x10: Minus_16; Mute 0x11: Minus_15; -15dB

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
17:15	CENTERSMSO	R/W	0x0	CENTER smartsound: Predefined bass/treble settings
23:18	RSD_23To18	R/W	0x00	Not used, must be fixed to '0'
Offset 0x8C	***SURROUND_TON_CON_REG0***			
4:0	SURROUNDBASS	R/W	0x00	SURROUND bass: (+15..-16dB, 1 dB steps) 15 = +15 dB .. -16 = -16 dB 1111: V15; +15 dB 0x10: Minus_16; -16 dB
9:5	SURROUNDTREB	R/W	0x00	SURROUND treble: (+15..-16dB, 1 dB steps) 15 = +15 dB .. -16 = -16 dB 1111: V15; +15 dB 0x10: Minus_16; -16 dB
12:10	SURROUNDSMSO	R/W	0x0	SURROUND smartsound: Predefined bass/treble settings
23:13	RSD_23To13	R/W	0x000	Not used, must be fixed to '0'
Offset 0x90	***AUX1_TON_CON_REG0***			
4:0	AUX1BASS	R/W	0x00	AUX1 bass: (+15..-16dB, 1 dB steps) 15 = +15 dB .. -16 = -16 dB 1111: V15; +15 dB 0x10: Minus_16; -16 dB
9:5	AUX1TREB	R/W	0x00	AUX1 treble: (+15..-16dB, 1 dB steps) 15 = +15 dB .. -16 = -16 dB 1111: V15; +15 dB 0x10: Minus_16; -16 dB
12:10	AUX1SMSO	R/W	0x0	AUX1: smartsound: Predefined bass/treble settings
23:13	RSD_23To13	R/W	0x000	Not used, must be fixed to '0'
Offset 0x94	***EQ_CONFIG_REG0***			
0	EQENABLE	R/W	0x0	EQ are functional in MAIN&CENTER channel 0: V0; disable EQ & enable Bass/Treble 1: V1; enable EQ & disable Bass/Treble
1	EQMAIN1MODE	R/W	0x0	Equaliser Main channel mode control for band1 0: V0; Graphic 1: V1; Parametric
2	EQMAIN2MODE	R/W	0x0	Equaliser Main channel mode control for band2 0: V0; Graphic 1: V1; Parametric
3	EQMAIN3MODE	R/W	0x0	Equaliser Main channel mode control for band3 0: V0; Graphic 1: V1; Parametric
4	EQMAIN4MODE	R/W	0x0	Equaliser Main channel mode control for band4 0: V0; Graphic 1: V1; Parametric

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
5	EQMAIN5MODE	R/W	0x0	Equaliser Main channel mode control for band5 0: V0; Graphic 1: V1; Parametric
6	EQMAIN1RELOAD	R/W	0x0	Reload Equalizer Main channel coefficients for band1 $0 = idle state $1 = reload coefficients after transition 0->1 $0->$1: Load coeff from cache array into work space. 0: V0; idle state 1: V1; reload coefficients after transition 0->1
7	EQMAIN2RELOAD	R/W	0x0	Reload Equalizer Main channel coefficients for band2 $0 = idle state $1 = reload coefficients after transition 0->1 $0->$1: Load coeff from cache array into work space. 0: V0; idle state 1: V1; reload coefficients after transition 0->1
8	EQMAIN3RELOAD	R/W	0x0	Reload Equalizer Main channel coefficients for band3 $0 = idle state $1 = reload coefficients after transition 0->1 $0->$1: Load coeff from cache array into work space. 0: V0; idle state 1: V1; reload coefficients after transition 0->1
9	EQMAIN4RELOAD	R/W	0x0	Reload Equalizer Main channel coefficients for band4 $0 = idle state $1 = reload coefficients after transition 0->1 $0->$1: Load coeff from cache array into work space. 0: V0; idle state 1: V1; reload coefficients after transition 0->1
10	EQMAIN5RELOAD	R/W	0x0	Reload Equalizer Main channel coefficients for band5 $0 = idle state $1 = reload coefficients after transition 0->1 $0->$1: Load coeff from cache array into work space. 0: V0; idle state 1: V1; reload coefficients after transition 0->1
11	EQCENTER1MODE	R/W	0x0	Equaliser Center channel control for band1 0: V0; Graphic 1: V1; Parametric
12	EQCENTER2MODE	R/W	0x0	Equaliser Center channel control for band2 0: V0; Graphic 1: V1; Parametric
13	EQCENTER3MODE	R/W	0x0	Equaliser Center channel control for band3 0: V0; Graphic 1: V1; Parametric
14	EQCENTER4MODE	R/W	0x0	Equaliser Center channel control for band4 0: V0; Graphic 1: V1; Parametric
15	EQCENTER5MODE	R/W	0x0	Equaliser Center channel control for band5 0: V0; Graphic 1: V1; Parametric

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
16	EQCENTER1RELOAD	R/W	0x0	Reload Equalizer Center channel coefficients for band1 $0 = idle state $1 = reload coefficients after transition 0->1 $0->$1: Load coeff from cache array into work space. 0: V0; idle state 1: V1; reload coefficients after transition 0->1
17	EQCENTER2RELOAD	R/W	0x0	Reload Equalizer Center channel coefficients for band2 $0 = idle state $1 = reload coefficients after transition 0->1 $0->$1: Load coeff from cache array into work space. 0: V0; idle state 1: V1; reload coefficients after transition 0->1
18	EQCENTER3RELOAD	R/W	0x0	Reload Equalizer Center channel coefficients for band3 $0 = idle state $1 = reload coefficients after transition 0->1 $0->$1: Load coeff from cache array into work space. 0: V0; idle state 1: V1; reload coefficients after transition 0->1
19	EQCENTER4RELOAD	R/W	0x0	Reload Equalizer Center channel coefficients for band4 $0 = idle state $1 = reload coefficients after transition 0->1 $0->$1: Load coeff from cache array into work space. 0: V0; idle state 1: V1; reload coefficients after transition 0->1
20	EQCENTER5RELOAD	R/W	0x0	Reload Equalizer Center channel coefficients for band5 $0 = idle state $1 = reload coefficients after transition 0->1 $0->$1: Load coeff from cache array into work space. 0: V0; idle state 1: V1; reload coefficients after transition 0->1
23:21	RSD_23To21	R/W	0x0	Not used, must be fixed to '0'
Offset 0x98	***EQMAINBAND1_COEF_REG0***			
4:0	EQMAINADRB1	R/W	0x00	Equalizer Main Channel Band1 (Address) Only used if EQMAINMODE = 1
11:5	RSD_11To5	R/W	0x00	0
23:12	EQMAINCOEFB1	R/W	0x000	Equalizer Main Channel Band1 (Coefficients) Only used if EQMAINMODE = 1
Offset 0x9C	***EQMAINBAND2_COEF_REG0***			
4:0	EQMAINADRB2	R/W	0x00	Equalizer Main Channel Band2 (Address) Only used if EQMAINMODE = 1
11:5	RSD_11To5	R/W	0x00	0
23:12	EQMAINCOEFB2	R/W	0x000	Equalizer Main Channel Band2 (Coefficients) Only used if EQMAINMODE = 1
Offset 0xA0	***EQMAINBAND3_COEF_REG0***			
4:0	EQMAINADRB3	R/W	0x00	Equalizer Main Channel Band3 (Address) Only used if EQMAINMODE = 1
11:5	RSD_11To5	R/W	0x00	0
23:12	EQMAINCOEFB3	R/W	0x000	Equalizer Main Channel Band3 (Coefficients) Only used if EQMAINMODE = 1

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
Offset 0xA4	***EQMAINBAND4_COEF_REG0***			
4:0	EQMAINADRB4	R/W	0x00	Equalizer Main Channel Band4 (Address) Only used if EQMAINMODE = 1
11:5	RSD_11To5	R/W	0x00	0
23:12	EQMAINCOEFB4	R/W	0x000	Equalizer Main Channel Band4 (Coefficients) Only used if EQMAINMODE = 1
Offset 0xA8	***EQMAINBAND5_COEF_REG0***			
4:0	EQMAINADRB5	R/W	0x00	Equalizer Main Channel Band5 (Address) Only used if EQMAINMODE = 1
11:5	RSD_11To5	R/W	0x00	0
23:12	EQMAINCOEFB5	R/W	0x000	Equalizer Main Channel Band5 (Coefficients) Only used if EQMAINMODE = 1
Offset 0xAC	***EQCENTERBAND1_COEF_REG0***			
4:0	EQCENTERADRB1	R/W	0x00	Equalizer CENTER Channel Band1 (Address) Only used if EQCENTERMODE = 1
11:5	RSD_11To5	R/W	0x00	0
23:12	EQCENTERCOEFB1	R/W	0x000	Equalizer CENTER Channel Band1 (Coefficients) Only used if EQCENTERMODE = 1
Offset 0xB0	***EQCENTERBAND2_COEF_REG0***			
4:0	EQCENTERADRB2	R/W	0x00	Equalizer CENTER Channel Band2 (Address) Only used if EQCENTERMODE = 1
11:5	RSD_11To5	R/W	0x00	0
23:12	EQCENTERCOEFB2	R/W	0x000	Equalizer CENTER Channel Band2 (Coefficients) Only used if EQCENTERMODE = 1
Offset 0xB4	***EQCENTERBAND3_COEF_REG0***			
4:0	EQCENTERADRB3	R/W	0x00	Equalizer CENTER Channel Band3 (Address) Only used if EQCENTERMODE = 1
11:5	RSD_11To5	R/W	0x00	0
23:12	EQCENTERCOEFB3	R/W	0x000	Equalizer CENTER Channel Band3 (Coefficients) Only used if EQCENTERMODE = 1
Offset 0xB8	***EQCENTERBAND4_COEF_REG0***			
4:0	EQCENTERADRB4	R/W	0x00	Equalizer CENTER Channel Band4 (Address) Only used if EQCENTERMODE = 1
11:5	RSD_11To5	R/W	0x00	0
23:12	EQCENTERCOEFB4	R/W	0x000	Equalizer CENTER Channel Band4 (Coefficients) Only used if EQCENTERMODE = 1
Offset 0xBC	***EQCENTERBAND5_COEF_REG0***			
4:0	EQCENTERADRB5	R/W	0x00	Equalizer CENTER Channel Band5 (Address) Only used if EQCENTERMODE = 1
11:5	RSD_11To5	R/W	0x00	0
23:12	EQCENTERCOEFB5	R/W	0x000	Equalizer CENTER Channel Band5 (Coefficients) Only used if EQCENTERMODE = 1

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
Offset 0xC0	***EQMAIN1_TON_CON_REG0***			
4:0	EQCHM1	R/W	0x00	Equalizer MAIN Channel Band 1 (100 Hz) 12 = +12dB .. -12 = -12dB 1100: V12; +12dB 0x14: Minus_12; -12dB
9:5	EQCHM2	R/W	0x00	Equalizer MAIN Channel Band 2 (300 Hz) 12 = +12dB .. -12 = -12dB 1100: V12; +12dB 0x14: Minus_12; -12dB
14:10	EQCHM3	R/W	0x00	Equalizer MAIN Channel Band 3 (1000 Hz) 12 = +12dB .. -12 = -12dB 1100: V12; +12dB 0x14: Minus_12; -12dB
23:15	RSD_23To15	R/W	0x000	Not used, must be fixed to '0'
Offset 0xC4	***EQMAIN2_TON_CON_REG0***			
4:0	EQCHM4	R/W	0x00	Equalizer MAIN Channel Band 4 (3000 Hz) 12 = +12dB .. -12 = -12dB 1100: V12; +12dB 0x14: Minus_12; -12dB
9:5	EQCHM5	R/W	0x00	Equalizer MAIN Channel Band 5 (8000 Hz) 12 = +12dB .. -12 = -12dB 1100: V12; +12dB 0x14: Minus_12; -12dB
23:10	RSD_23To10	R/W	0x0000	Not used, must be fixed to '0'
Offset 0xC8	***EQCENTER1_TON_CON_REG0***			
4:0	EQCHC1	R/W	0x00	Equalizer CENTER Channel Band 1 (100 Hz) 12 = +12dB .. -12 = -12dB 1100: V12; +12dB 0x14: Minus_12; -12dB
9:5	EQCHC2	R/W	0x00	Equalizer CENTER Channel Band 2 (300 Hz) 12 = +12dB .. -12 = -12dB 1100: V12; +12dB 0x14: Minus_12; -12dB
14:10	EQCHC3	R/W	0x00	Equalizer CENTER Channel Band 3 (1000 Hz) 12 = +12dB .. -12 = -12dB 1100: V12; +12dB 0x14: Minus_12; -12dB
23:15	RSD_23To15	R/W	0x000	Not used, must be fixed to '0'
Offset 0xCC	***EQCENTER2_TON_CON_REG0***			
4:0	EQCHC4	R/W	0x00	Equalizer CENTER Channel Band 4 (3000 Hz) 12 = +12dB .. -12 = -12dB 1100: V12; +12dB 0x14: Minus_12; -12dB

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
9:5	EQCHC5	R/W	0x00	Equalizer CENTER Channel Band 5 (8000 Hz) 12 = +12dB .. -12 = -12dB 1100: V12; +12dB 0x14: Minus_12; -12dB
23:10	RSD_23To10	R/W	0x0000	Not used, must be fixed to '0'
Offset 0xD0	***MON_SEL_REG0***			
4:0	ASMOCP1	R/W	0x01	OUTPUT SELECTION for OUTCOPY1 $0 = MAIN/L CHANNEL $1 = MAIN/R CHANNEL $2 = SUB CHANNEL $3 = C CHANNEL $4 = SL CHANNEL $5 = SR CHANNEL $6 = AUX1L CHANNEL $7 = AUX1R CHANNEL $8 = AUX2L CHANNEL $9 = AUX2R CHANNEL $A = AUX3L CHANNEL $B = AUX3R CHANNEL $C = AUX4L CHANNEL $D = AUX4R CHANNEL $E = AUX5 L CHANNEL $F = AUX5 R CHANNEL $10 = AUX6 L CHANNEL $11 = AUX6 R CHANNEL $12 = Main Sum CHANNEL >$12 = reserved 0: V0; MAIN/L CHANNEL 1: V1; MAIN/R CHANNEL 10: V2; SUB CHANNEL 11: V3; C CHANNEL 100: V4; SL CHANNEL 101: V5; SR CHANNEL 110: V6; AUX1L CHANNEL 111: V7; AUX1R CHANNEL 1000: V8; AUX2L CHANNEL 1001: V9; AUX2R CHANNEL 1010: VA; AUX3L CHANNEL 1011: VB; AUX3R CHANNEL 1100: VC; AUX4L CHANNEL 1101: VD; AUX4R CHANNEL 1110: VE; AUX5 L CHANNEL 1111: VF; AUX5 R CHANNEL 0x10: V10; AUX6 L CHANNEL 0x11: V11; AUX6 R CHANNEL 0x12: V12; Main Sum CHANNEL

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
9:5	ASMOCP2	R/W	0x00	OUTPUT SELECTION for OUTCOPY2 $0 = MAIN/L CHANNEL $1 = MAIN/R CHANNEL $2 = SUB CHANNEL $3 = C CHANNEL $4 = SL CHANNEL $5 = SR CHANNEL $6 = AUX1L CHANNEL $7 = AUX1R CHANNEL $8 = AUX2L CHANNEL $9 = AUX2R CHANNEL $A = AUX3L CHANNEL $B = AUX3R CHANNEL $C = AUX4L CHANNEL $D = AUX4R CHANNEL $E = AUX5 L CHANNEL $F = AUX5 R CHANNEL $10 = AUX6 L CHANNEL $11 = AUX6 R CHANNEL $12 = Main Sum CHANNEL >$12 = reserved 0: V0; MAIN/L CHANNEL 1: V1; MAIN/R CHANNEL 10: V2; SUB CHANNEL 11: V3; C CHANNEL 100: V4; SL CHANNEL 101: V5; SR CHANNEL 110: V6; AUX1L CHANNEL 111: V7; AUX1R CHANNEL 1000: V8; AUX2L CHANNEL 1001: V9; AUX2R CHANNEL 1010: VA; AUX3L CHANNEL 1011: VB; AUX3R CHANNEL 1100: VC; AUX4L CHANNEL 1101: VD; AUX4R CHANNEL 1110: VE; AUX5 L CHANNEL 1111: VF; AUX5 R CHANNEL 0x10: V10; AUX6 L CHANNEL 0x11: V11; AUX6 R CHANNEL 0x12: V12; Main Sum CHANNEL

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
14:10	AUDIOMONSS	R/W	0x00	SIGNAL SOURCE AUDIO MONITOR 0: V00; DEC 1: V01; Mono 10: V02; SAP 11: V03; PIPMONO 100: V04; ADC1 101: V05; Noise Generator 110: V06; Outcopy 111: V07; IIS 1.1 1.2 1000: V08; IIS 1.1 2.1 1001: V09; IIS 1.1 2.2 1010: V0A; IIS 1.1 3.1 1011: V0B; IIS 1.1 3.2 1100: V0C; IIS 1.1 4.1 1101: V0D; IIS 1.1 4.2 1110: V0E; IIS 1.2 2.1 1111: V0F; IIS 1.2 2.2 0x10: V10; IIS 1.2 3.1 0x11: V11; IIS 1.2 3.2 0x12: V12; IIS 1.2 4.1 0x13: V13; IIS 1.2 4.2 0x14: V14; IIS 2.1 2.2 0x15: V15; IIS 2.1 3.1 0x16: V16; IIS 2.1 3.2 0x17: V17; IIS 2.2 3.1 0x18: V18; IIS 2.2 3.2 0x19: V19; IIS 3.1 3.2 0x1A: V1A; IIS 4.1 4.2 0x1B: V1B; IIS 5.1 5.2 0x1C: V1C; IIS 6.1 6.2 0x1D: V1D; Digital Silence 0x1E: V1E; Reserved 0x1F: V1F; Reserved
17:15	AUDIOMONDM	R/W	0x0	DIGITAL MATRIX AUDIO MONITOR 0: V0; AB [Stereo] (automatrix off) 1: V1; (A+B)/2 [Mono] (automatrix off) 10: V2; AA [Lang. A] (automatrix off) 11: V3; BB [Lang. B] (automatrix off) 100: V4; BA [Swap] (automatrix off) 101: V5; (A-B)/2 Differential Signal for stereo detection (automatrix off) 110: V6; Language A (automatrix on) 111: V7; Language B (automatrix on)

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
19:18	AUDIOMONMODE	R/W	0x0	Audio Monitor Mode 0: V0; LAST SAMPLE 1: V1; PEAK DETECTOR 10: V2; QUASI PEAK DETECTOR
23:20	RSD_23To20	R/W	0x0	reserved
Offset 0xD4	***MPI_CONTROL_REG0***			
7:0	AUDMPIDIV	R/W	0x01	MPI rate divider, MPI rate = 53 kHz / MPIDIV. If 0, selects highest possible MPI rate (k*53 kHz tbf)
8	NSPD_N	R/W	0x1	Noise Shaper PowerDown 0: V0; PowerDown 1: V1; PowerUp
23:9	RSD_23To9	R/W	0x0000	reserved
Offset 0xD8	***ACC_MAINCH_REG0***			
23:12	ACCMAINCOEF	R/W	0x000	ACC main channel coefficients
7:0	ACCMAINADR	R/W	0x00	ACC main channel coefficient address
11:8	RSD_11To8	R/W	0x0	Reserved
Offset 0xDC	***ACC_CENTERCH_REG0***			
7:0	ACCCENTERADR	R/W	0x00	ACC center channel coefficient address
11:8	RSD_11To8	R/W	0x0	Reserved
23:12	ACCCENTERCOEF	R/W	0x000	ACC center channel coefficients
Offset 0xE0	***AS_CONTROL_REG0***			
1:0	ACS_NrSpeakers	R/W	0x0	Speaker System 0: V0; 5 Speaker application 1: V1; 3 Speaker application
4:2	ACS_MODE	R/W	0x0	Active Surround Effect Strength 0: V0; Maximum 1: V1; Natural 10: V2; Reserved 11: V3; Off
7:5	ACS_FadeTime	R/W	0x5	Active Surround Fade Time 0: V0; 0.5 sec 1: V1; 0.6 sec 10: V2; 0.75 sec 11: V3; 1.0 sec 100: V4; 1.2 sec 101: V5; 1.5 sec 110: V6; 2.0 sec 111: V7; 3.0 sec
23:8	RSD_23To8	R/W	0x0000	Reserved

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
Offset 0xE4	***AS_PMC_TRIM_REG0***			
4:0	ACS_PMCScaleF	R/W	0x06	Trim PMC Output Level, Main Left, Right 0: V00; +6dB 1: V01; +5dB 10: V02; +4dB 11: V03; +3dB 100: V04; +2dB 101: V05; +1dB 110: V06; 0dB 111: V07; -1dB 1000: V08; -2dB 1001: V09; -3dB 1010: V0A; -4dB 1011: V0B; -5dB 1100: V0C; -6dB 1101: V0D; -7dB 1110: V0E; -8dB 1111: V0F; -9dB 0x10: V10; -10dB 0x11: V11; -11dB 0x12: V12; -12dB 0x13: V13; -13dB 0x14: V14; -14dB 0x15: V15; -15dB 0x16: V16; -16dB 0x17: V17; -17dB 0x18: V18; -18dB 0x19: V19; -19dB 0x1A: V1A; -20dB 0x1B: V1B; -21dB 0x1C: V1C; -22dB 0x1D: V1D; -23dB 0x1E: V1E; -24dB 0x1F: V1F; -25dB

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
9:5	ACS_PMCScaleC	R/W	0x06	Trim PMC Output Level, Center 0: V00; +6dB 1: V01; +5dB 10: V02; +4dB 11: V03; +3dB 100: V04; +2dB 101: V05; +1dB 110: V06; 0dB 111: V07; -1dB 1000: V08; -2dB 1001: V09; -3dB 1010: V0A; -4dB 1011: V0B; -5dB 1100: V0C; -6dB 1101: V0D; -7dB 1110: V0E; -8dB 1111: V0F; -9dB 0x10: V10; -10dB 0x11: V11; -11dB 0x12: V12; -12dB 0x13: V13; -13dB 0x14: V14; -14dB 0x15: V15; -15dB 0x16: V16; -16dB 0x17: V17; -17dB 0x18: V18; -18dB 0x19: V19; -19dB 0x1A: V1A; -20dB 0x1B: V1B; -21dB 0x1C: V1C; -22dB 0x1D: V1D; -23dB 0x1E: V1E; -24dB 0x1F: V1F; -25dB

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
14:10	ACS_PMCScaleS	R/W	0x06	Trim PMC Output Level, Surround 0: V00; +6dB 1: V01; +5dB 10: V02; +4dB 11: V03; +3dB 100: V04; +2dB 101: V05; +1dB 110: V06; 0dB 111: V07; -1dB 1000: V08; -2dB 1001: V09; -3dB 1010: V0A; -4dB 1011: V0B; -5dB 1100: V0C; -6dB 1101: V0D; -7dB 1110: V0E; -8dB 1111: V0F; -9dB 0x10: V10; -10dB 0x11: V11; -11dB 0x12: V12; -12dB 0x13: V13; -13dB 0x14: V14; -14dB 0x15: V15; -15dB 0x16: V16; -16dB 0x17: V17; -17dB 0x18: V18; -18dB 0x19: V19; -19dB 0x1A: V1A; -20dB 0x1B: V1B; -21dB 0x1C: V1C; -22dB 0x1D: V1D; -23dB 0x1E: V1E; -24dB 0x1F: V1F; -25dB
23:15	RSD_23To15	R/W	0x000	Reserved

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
Offset 0xE8	***AS_IMONO_LFE_TRIM_REG0***			
4:0	ACS_IM2ScaleF	R/W	0x0C	Trim IMono2 Output Level - Front channels 0: V00; +12dB 1: V01; +11dB 10: V02; +10dB 11: V03; +9dB 100: V04; +8dB 101: V05; +7dB 110: V06; +6dB 111: V07; +5dB 1000: V08; +4dB 1001: V09; +3dB 1010: V0A; +2dB 1011: V0B; +1dB 1100: V0C; 0dB 1101: V0D; -1dB 1110: V0E; -2dB 1111: V0F; -3dB 0x10: V10; -4dB 0x11: V11; -5dB 0x12: V12; -6dB 0x13: V13; -7dB 0x14: V14; -8dB 0x15: V15; -9dB 0x16: V16; -10dB 0x17: V17; -11dB 0x18: V18; -12dB 0x19: V19; -13dB 0x1A: V1A; -14dB 0x1B: V1B; -15dB 0x1C: V1C; -16dB 0x1D: V1D; -17dB 0x1E: V1E; -18dB 0x1F: V1F; -19dB

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
9:5	ACS_IM2ScaleC	R/W	0x0C	Trim IMono2 Output Level - Center Channel 0: V00; +12dB 1: V01; +11dB 10: V02; +10dB 11: V03; +9dB 100: V04; +8dB 101: V05; +7dB 110: V06; +6dB 111: V07; +5dB 1000: V08; +4dB 1001: V09; +3dB 1010: V0A; +2dB 1011: V0B; +1dB 1100: V0C; 0dB 1101: V0D; -1dB 1110: V0E; -2dB 1111: V0F; -3dB 0x10: V10; -4dB 0x11: V11; -5dB 0x12: V12; -6dB 0x13: V13; -7dB 0x14: V14; -8dB 0x15: V15; -9dB 0x16: V16; -10dB 0x17: V17; -11dB 0x18: V18; -12dB 0x19: V19; -13dB 0x1A: V1A; -14dB 0x1B: V1B; -15dB 0x1C: V1C; -16dB 0x1D: V1D; -17dB 0x1E: V1E; -18dB 0x1F: V1F; -19dB

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
14:10	ACS_IM2ScaleS	R/W	0x0C	Trim IMono2 Output Level - Suround Channel 0: V00; +12dB 1: V01; +11dB 10: V02; +10dB 11: V03; +9dB 100: V04; +8dB 101: V05; +7dB 110: V06; +6dB 111: V07; +5dB 1000: V08; +4dB 1001: V09; +3dB 1010: V0A; +2dB 1011: V0B; +1dB 1100: V0C; 0dB 1101: V0D; -1dB 1110: V0E; -2dB 1111: V0F; -3dB 0x10: V10; -4dB 0x11: V11; -5dB 0x12: V12; -6dB 0x13: V13; -7dB 0x14: V14; -8dB 0x15: V15; -9dB 0x16: V16; -10dB 0x17: V17; -11dB 0x18: V18; -12dB 0x19: V19; -13dB 0x1A: V1A; -14dB 0x1B: V1B; -15dB 0x1C: V1C; -16dB 0x1D: V1D; -17dB 0x1E: V1E; -18dB 0x1F: V1F; -19dB

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
19:15	ACS_OutSelScaleLFE	R/W	0x00	Trim LFE Output Level 0: V00; 0dB 1: V01; -1dB 10: V02; -2dB 11: V03; -3dB 100: V04; -4dB 101: V05; -5dB 110: V06; -6dB 111: V07; -7dB 1000: V08; -8dB 1001: V09; -9dB 1010: V0A; -10dB 1011: V0B; -11dB 1100: V0C; -12dB 1101: V0D; -13dB 1110: V0E; -14dB 1111: V0F; -15dB 0x10: V10; -16dB 0x11: V11; -17dB 0x12: V12; -18dB 0x13: V13; -19dB 0x14: V14; -20dB 0x15: V15; -21dB 0x16: V16; -22dB 0x17: V17; -23dB 0x18: V18; -24dB 0x19: V19; -25dB 0x1A: V1A; -26dB 0x1B: V1B; -27dB 0x1C: V1C; -28dB 0x1D: V1D; -29dB 0x1E: V1E; -30dB 0x1F: V1F; -31dB
23:20	RSD_23To20	R/W	0x0	Reserved

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
Offset 0xEC	***AS_SIGNALSTATUS_REG0***			
3:0	ACS_SpeechProbability	R	0x0	Speech Probability 0: V0; 0%...6% 1: V1; 6%...13% 10: V2; 13%...19% 11: V3; 19%...25% 100: V4; 25%...31% 101: V5; 31%...38% 110: V6; 38%...44% 111: V7; 44%...50% 1000: V8; 50%...56% 1001: V9; 56%...63% 1010: VA; 63%...69% 1011: VB; 69%...75% 1100: VC; 75%...81% 1101: VD; 81%...88% 1110: VE; 88%...94% 1111: VF; 94%...100%
7:4	ACS_MonoProbability	R	0x0	Mono Probability 0: V0; 0%...6% 1: V1; 6%...13% 10: V2; 13%...19% 11: V3; 19%...25% 100: V4; 25%...31% 101: V5; 31%...38% 110: V6; 38%...44% 111: V7; 44%...50% 1000: V8; 50%...56% 1001: V9; 56%...63% 1010: VA; 63%...69% 1011: VB; 69%...75% 1100: VC; 75%...81% 1101: VD; 81%...88% 1110: VE; 88%...94% 1111: VF; 94%...100%

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
11:8	ACS_SignalClass	R	0x0	Signal Status 0: V0; Reserved 1: V1; Mono and Speech 10: V2; Mono and Music 11: V3; Poor Stereo and Speech 100: V4; Poor Stereo and Music 101: V5; Good Stereo and Speech 110: V6; Good Stereo and Music 111: V7; Reserved
23:12	RSD_23To12	R	0x000	Reserved
Offset 0xF0	***AS_STATUS1_REG0***			
3:0	ACS_Status_IMono2_Center	R	0x0	Sub-Module Status, IMono2-Center 0: V0; Not Active 1111: VF; Active
7:4	ACS_Status_StereoPP	R	0x0	Sub-Module Status, Stereo plus plus 0: V0; Not Active 1111: VF; Active
11:8	ACS_Status_PMC	R	0x0	Sub-Module Status, PMC 0: V0; Not Active 1111: VF; Active
15:12	ACS_Status_IMono2	R	0x0	Sub-Module Status, IMono2 0: V0; Not Active 1111: VF; Active
19:16	ACS_Status_IStereo	R	0x0	Sub-Module Status, IStereo 0: V0; Not Active 1111: VF; Active
23:20	RSD_23To20	R	0x0	Reserved
Offset 0xF4	***AS_STATUS2_REG0***			
3:0	ACS_Status_Candeo_Center	R	0x0	Sub-Module Status, Candeo Center 0: V0; Not Active 1111: VF; Active
7:4	ACS_Status_Candeo_Surround	R	0x0	Sub-Module Status, Candeo Surround 0: V0; Not Active 1111: VF; Active
11:8	ACS_Status_FrontMute	R	0x0	Output Channel Status Front 0: V0; Muted 1111: VF; Un-Muted
15:12	ACS_Status_CenterMute	R	0x0	Output Channel Status Center 0: V0; Muted 1111: VF; Un-Muted

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
19:16	ACS_Status_SurroundMute	R	0x0	Output Channel Status Surround 0: V0; Muted 1111: VF; Un-Muted
23:20	RSD_23To20	R	0x0	Reserved
Offset 0xF8	***DPL2_MM_CON_REG0***			
0	DPL2_Panorama	R/W	0x0	DPL2 Music Panorama Mode 0: V0; Not Active 1: V1; Active
3:1	DPL2_DimCtrl	R/W	0x0	DPL2 Dimension Control in Music Mode 0: V0; 100% Back 1: V1; 66% Back 10: V2; 33% Back 11: V3; Normal 100: V4; 33% Front 101: V5; 66% Front 110: V6; 100% Front 111: V7; Reserved
6:4	DPL2_CenterCtrl	R/W	0x0	DPL2 Center Width Control in Music Mode 0: V0; 100% Center 1: V1; 86% Center 10: V2; 71% Center 11: V3; 57% Center 100: V4; 43% Center 101: V5; 28% Center 110: V6; 14% Center 111: V7; 0% Center
23:7	RSD_23To7	R/W	0x00000	Reserved
Offset 0x180A8	***SND_AD_STATUS00***			
23:0	See_INF_AUD_LEV_MON_REG	R	0x000000	copy of INF_AUD_LEV_MON_REG, suitable for fast access
31:24	RSD_31To24	R	0x00	not used

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
Offset 0x180B4	***SND_AD_T020***			
8:0	DEBUG_CNTRL	R/W	0x000	Debug control [8..0] Input Output 0 0000 0000 No Input selected No Output selected 0 0001 0001 Mixer in SIF 8 bit Mixer out SIF 8 bit 0 0010 0010 Mixer in Audio 8bit Mixer out Audio 8 bit 0 0011 0011 NICAM in PCLK and DATA NICAM out PCLK and DATA 0 0100 0100 NOISESHAPER in 1, 5, 9 a 4 bit NOISESHAPER out 1, 5, 9 a 4 bit 0 0101 0101 NOISESHAPER in 2, 6, 10 a 4 bit NOISESHAPER out 2, 6, 10 a 4 bit 0 0110 0110 NOISESHAPER in 3, 7, 11 a 4 bit NOISESHAPER out 3, 7, 11 a 4 bit 0 0111 0111 NOISESHAPER in 4, 8, 12 a 4 bit NOISESHAPER out 4, 8, 12 a 4 bit 0 1000 1000 SDI 12bit SDI 12bit 0 1001 1001 SDO 12bit SDO 12bit 0 1010 1010 DTL 8bit DTL 8bit 1 1xxx x000 No Functionality FM/BTSC incl enable,one 1 1xxx x001 FM/BTSCincl enable,two 1 1xxx x010 Japan mainchannel incl enable,one 1 1xxx x011 Japan subchannel incl enable,two 1 1xxx x100 NICAM incl enable,one 1 1xxx x101 NICAM incl enable,two 1 1xxx x110 ADC incl enable,one 1 1xxx x111 ADC incl enable,two
9	PI_BYPASS_SCAN	R/W	0x0	Bypass testrail during debugmode disable
14:10	RSD_14To10	R	0x00	reserved
22:15	EIR_BUS_H	R/W	0x00	EIR_BUS[31:24]
23	TCB_GOTO_MODE	R/W	0x0	Enable bit for goto mode. The goto mode is a mode in which an instruction can be forced onto the Epics7 instruction bus. The instruction is stored in a register in the Test Control Block (TCB) and is usually a goto instruction to force the DSP to jump to a certain routine in program memory which will never be accessed in functional mode. These routines can be used as test/evaluation routines.
31:24	RSD_31To24	R	0x00	not used
Offset 0x180B8	***SND_AD_T010***			
23:0	EIR_BUS_L	R/W	0x000000	EIR_BUS[23:0]
31:24	RSD_31To24	R	0x00	not used
Offset 0x180BC	***SND_AD_M000***			
0	BIOPRASEL	R/W	0x0	BIOS / program RAM select 0: V0; program RAM 1: V1; BIOS
1	PRAPROSEL	R/W	0x0	program RAM / ROM select 0: V0; program ROM select 1: V1; program RAM select
2	PC_RESET_MPI	R/W	0x0	program counter reset for AUDIO DSP 0: V0; no reset 1: V1; reset
3	IIC_INT	R/W	0x0	EMMI flag to EPICS 0: V0; no set 1: V1; set

Table 2: AUDIO_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
4	BAM_EN	R/W	0x0	bus allocation minimizer enable 0: V0; disabled 1: V1; enabled
6:5	I2S_FORMAT	R/W	0x0	IIS format control 0: V0; Philips 1: V1; Sony 10: V2; Japanese 24 bit 11: V3; Japanese 24 bit
23:7	RSD_23To7	R/W	0x00000	reserved
31:24	RSD_31To24	R	0x00	not used
Offset 0x3FFE0	***SND_AD_INT_STATUS0***			
23:0	RSD_23To0	R	0x000000	reserved
24	TNSACT_GRANT	R	0x0	indicates a pending interrupt caused to inform the DTL initiator that a new transactions on a high latency software control register will be granted (alias: RTF = Ready for Transfer Flag) 0: V0; not pending 1: V1; pending
31:25	RSD_31To25	R	0x00	not used
Offset 0x3FFE4	***SND_AD_INT_ENABLE0***			
24:0	EN_INT_COND	R/W	0x0000000	enable interrupt request condition INT_COND[i] 0: V0; disabled 1: V1; enabled
31:25	RSD_31To25	R	0x00	not used
Offset 0x3FFE8	***SND_AD_INT_CLEAR0***			
24:0	CLR_INT_COND	W	0x0000000	clear interrupt request condition SND_AD_INT_STATUS[i] 0: V0; preserve old state 1: V1; clear
31:25	RSD_31To25	W	0x00	not used
Offset 0x3FFEC	***SND_AD_INT_SET0***			
24:0	SET_INT_COND	W	0x0000000	set interrupt request condition SND_AD_INT_STATUS[i], for debug purposes 0: V0; preserve old state 1: V1; set
31:25	RSD_31To25	W	0x00	not used
Offset 0x3FFFC	***SND_AD_MOD_ID0***			
7:0	APERTURE	R	0x3F	index for aperture size in global memory map (= aperture_size/4K -1)
11:8	MINOR_REV	R	0x0	Minor revision sound core
15:12	MAJOR_REV	R	0x0	Major revision sound core
31:16	ID	R	0xA067	Module identifier sound core

Chapter 3: DCU Registers

PNX2000

Rev. 01 — 15 December 2003

1. DCU Register Descriptions

Table 1: DCU Register Summary

Offset	Name	Description
0x0	DCR1	Data capture control register 1
0x4	LCR2_5	Line Control Registers 2 to 5
0x8	LCR6_9	Line Control Registers 6 to 9
0xC	LCR10_13	Line Control Registers 10 to 13
0x10	LCR14_17	Line Control Registers 14 to 17
0x14	LCR18_21	Line Control Registers 18 to 21
0x18	LCR22_24	Line Control Registers 22 to 24
0x1C	DCS	Data Capture Status
0x2C	DCR2	Data Capture Register 2
0xFCC	Debug_Ctrl	Debug Control Register
0xFE0	INT_STATUS	Interrupt Status
0xFE4	INT_ENABLE	Interrupt Enable
0xFE8	INT_CLEAR	Interrupt Clear
0xFEC	INT_SET	Interrupt Set
0xFFC	MOD_ID	Module ID

Table 2: DCU Registers

Bit	Symbol	Access	Reset Value	Description
Offset 0x0	*DCR1*			
31	INV_MSB	R/W	0x0	Invert MSB of incoming CVBS data (used for signed data). '0' = no invert; '1' = invert MSB
30:22	V	R/W	0x000	Vertical position of CVFLD interrupt, start of line number 1-312 (must be non-zero for interrupt to be issued)
21:16	H	R/W	0x00	Horizontal position of packet received interrupt, in microseconds (32-63, 0-3)
15:8	FC	R/W	0x00	Framing code for 'open' data types
7	DPH	R/W	0x0	'0' = do not decode page header; '1' = hamming 8/4 decode page header (bytes 6 to 13 of packets X/0). This also requires DMP to be set.
6	DMP	R/W	0x0	'0' = do not decode magazine and packet; '1' = decode magazine and packet (hamming 8/4)

Table 2: DCU Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
5	HAM_DISABLE	R/W	0x0	'0' = hamming check magazine and packet address of open data types; '1' = do not hamming check. Hamming checking is only optional for data types 8 to F
4	FCE	R/W	0x0	'0' = one error allowed in framing code; '1' = no errors allowed in framing code
3	VID_525	R/W	0x0	'0' = expect 625 line transmissions; '1' = expect 525 line transmissions
2	HUNT_DISABLE	R/W	0x0	'0' = amplitude searching allowed; '1' = amplitude searching disabled. Amplitude searching should not be disabled in normal operation.
1	VCR	R/W	0x0	'0' = normal PLL mode (no integral path); '1' = VCR PLL mode (integral path enabled)
0	ACQ_EN	R/W	0x0	'0' = All lines treated as 'do-not-acquire'; '1' = normal acquisition mode
Offset 0x4	***LCR2_5***			
23:20	L4F1_DT	R/W	0x0	Data Type for Line 4, Field 1.
19:16	L4F2_DT	R/W	0x0	Data Type for Line 4, Field 2.
15:12	L3F1_DT	R/W	0x0	Data Type for Line 3, Field 1.
11:8	L3F2_DT	R/W	0x0	Data Type for Line 3, Field 2.
7:4	L2F1_DT	R/W	0x0	Data Type for Line 2, Field 1.
3:0	L2F2_DT	R/W	0x0	Data Type for Line 2, Field 2.
31:28	L5F1_DT	R/W	0x0	Data Type for Line 5, Field 1.
27:24	L5F2_DT	R/W	0x0	Data Type for Line 5, Field 2.
Offset 0x8	***LCR6_9***			
31:28	L9F1_DT	R/W	0x0	Data Type for Line 9, Field 1.
27:24	L9F2_DT	R/W	0x0	Data Type for Line 9, Field 2.
23:20	L8F1_DT	R/W	0x0	Data Type for Line 8, Field 1.
19:16	L8F2_DT	R/W	0x0	Data Type for Line 8, Field 2.
15:12	L7F1_DT	R/W	0x0	Data Type for Line 7, Field 1.
11:8	L7F2_DT	R/W	0x0	Data Type for Line 7, Field 2.
7:4	L6F1_DT	R/W	0x0	Data Type for Line 6, Field 1.
3:0	L6F2_DT	R/W	0x0	Data Type for Line 6, Field 2.
Offset 0xC	***LCR10_13***			
31:28	L13F1_DT	R/W	0x0	Data Type for Line 13 Field 1.
27:24	L13F2_DT	R/W	0x0	Data Type for Line 13 Field 2.
23:20	L12F1_DT	R/W	0x0	Data Type for Line 12 Field 1.
19:16	L12F2_DT	R/W	0x0	Data Type for Line 12 Field 2.
15:12	L11F1_DT	R/W	0x0	Data Type for Line 11 Field 1.
11:8	L11F2_DT	R/W	0x0	Data Type for Line 11 Field 2.
7:4	L10F1_DT	R/W	0x0	Data Type for Line 10 Field 1.
3:0	L10F2_DT	R/W	0x0	Data Type for Line 10 Field 2.

Table 2: DCU Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
Offset 0x10	***LCR14_17***			
31:28	L17F1_DT	R/W	0x0	Data Type for Line 17, Field 1.
27:24	L17F2_DT	R/W	0x0	Data Type for Line 17, Field 2.
23:20	L16F1_DT	R/W	0x0	Data Type for Line 16, Field 1.
19:16	L16F2_DT	R/W	0x0	Data Type for Line 16, Field 2.
15:12	L15F1_DT	R/W	0x0	Data Type for Line 15, Field 1.
11:8	L15F2_DT	R/W	0x0	Data Type for Line 15, Field 2.
7:4	L14F1_DT	R/W	0x0	Data Type for Line 14, Field 1.
3:0	L14F2_DT	R/W	0x0	Data Type for Line 14, Field 2.
Offset 0x14	***LCR18_21***			
31:28	L21F1_DT	R/W	0x0	Data Type for Line 21, Field 1.
27:24	L21F2_DT	R/W	0x0	Data Type for Line 21, Field 2.
23:20	L20F1_DT	R/W	0x0	Data Type for Line 20, Field 1.
19:16	L20F2_DT	R/W	0x0	Data Type for Line 20, Field 2.
15:12	L19F1_DT	R/W	0x0	Data Type for Line 19, Field 1.
11:8	L19F2_DT	R/W	0x0	Data Type for Line 19, Field 2.
7:4	L18F1_DT	R/W	0x0	Data Type for Line 18, Field 1.
3:0	L18F2_DT	R/W	0x0	Data Type for Line 18, Field 2.
Offset 0x18	***LCR22_24***			
31:28	RSD_31To28	R	0x0	Reserved
27:24	RSD_27To24	R	0x0	Reserved
23:20	L24F1_DT	R/W	0xF	Data Type for Lines 24 and higher, Field 1.
19:16	L24F2_DT	R/W	0xF	Data Type for Lines 24 and higher, Field 2.
15:12	L23F1_DT	R/W	0x0	Data Type for Line 23, Field 1.
11:8	L23F2_DT	R/W	0x0	Data Type for Line 23, Field 2.
7:4	L22F1_DT	R/W	0x0	Data Type for Line 22, Field 1.
3:0	L22F2_DT	R/W	0x0	Data Type for Line 22, Field 2.
Offset 0x1C	***DCS***			
31	F2	R	0xX	Set to '1' at the start of field 2 of frame; set to '0' at the start of field 1. Field 1 is 'odd', field 2 is 'even'.
30:25	RSD_30To25	R	0x00	Reserved
24:16	LN	R	0xXXX	Line number in current field (1..313). Updated at the start of each line even if the data type is 'do not acquire'
15	FC8V	R	0xX	Teletext data received with no errors in framing code within last field
14	FC7V	R	0xX	Teletext data received with one error in framing code within last field
13	VPSV	R	0xX	Video Programming Signal (VPS) data received within last field
12	WSSV	R	0xX	WSS data received within last field

Table 2: DCU Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
11	CCV	R	0xX	CC data received within last field
10	RSD_Bit10	R	0x0	Reserved
9	RSD_Bit9	R/W	0x1	Reserved
8	DCS_525R	R	0xX	525-line transmission detect by acquisition line counter
7	DPH	R	0xX	Decoding of Page Headers enabled
6	DMP	R	0xX	Decoding of Magazine and Packet numbers enabled
5:4	RSD_5To4	R	0x0	Reserved
3:0	DT	R	0xX	Type of data received
Offset 0x2C	***DCR2***			
31:24	RSD_31To24	R	0x00	Reserved
23	WSS_CRC	R/W	0x0	WSS525 CRC control. '0' = WSS525 CRC check is ignored for packet validity checking ; '1' = WSS525 packet validity depends on result of CRC check.
22	INPUT_SEL	R/W	0x0	Video input selection 0: VideoInput_First; Selects first video (I2D) input stream 1: VideoInput_Second; Selects second video (I2D) input stream
21:18	RSD_21To18	R/W	0x0	Reserved
17	FPOS	R/W	0x0	Field Input Polarity Control 0: OddPolarityLow; Field input polarity 0 = odd, 1 = even 1: OddPolarityHigh; Field input polarity 0 = even, 1 = odd
16:8	VSPOS	R/W	0x000	Timing of vertical sync input relative to CVBS, in lines
7:0	HSPOS	R/W	0x00	Timing of horizontal sync input relative to CVBS, in increments of 0.25us (1/256 of line period)
Offset 0xFCC	***Debug_Ctrl***			
31:2	RSD_31To2	R	0x00000000	Reserved
1:0	DBG	R/W	0x0	Debug output multiplexer select
Offset 0xFE0	***INT_STATUS***			
31:2	RSD_31To2	R	0x00000000	Reserved
1	PKTRX_STATUS	R	0x0	Status of packet received interrupt
0	CVFLD_STATUS	R	0x0	Status of CVBS field sync interrupt
Offset 0xFE4	***INT_ENABLE***			
31:2	RSD_31To2	R	0x00000000	Reserved
1	PKTRX_ENABLE	R/W	0x0	Packet received interrupt enable
0	CVFLD_ENABLE	R/W	0x0	CVBS field sync interrupt enable
Offset 0xFE8	***INT_CLEAR***			
31:2	RSD_31To2	R/W	0x00000000	Reserved
1	PKTRX_CLEAR	W	0x0	Write '1' to clear named interrupt. Write '0' has no effect
0	CVFLD_CLEAR	W	0x0	Write '1' to clear named interrupt. Write '0' has no effect

Table 2: DCU Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
Offset 0xFEC	***INT_SET***			
31:2	RSD_31To2	R/W	0x00000000	Reserved
1	PKTRX_SET	W	0x0	Write '1' to set named interrupt. Write '0' has no effect
0	CVFLD_SET	W	0x0	Write '1' to set named interrupt. Write '0' has no effect
Offset 0xFFC	***MOD_ID***			
31:16	Id	R	0xA007	Module Identifier.
15:12	Major_rev	R	0x2	Major revision. Any revisions that may break software compatibility.
11:8	Minor_rev	R	0x0	Minor revision. Any revisions that still keep software compatibility.
7:0	Aperture	R	0x00	Aperture size. Encoded as (aperture size/4K)-1; so 0 means 4K (the default)

Chapter 4: DEMDEC_DSP Registers

PNX2000

Rev. 01 — 15 December 2003

1. DEMDEC_DSP Register Descriptions

Table 1: DEMDEC_DSP Register Summary

Offset	Name	Description
0x4	INF_MAIN_STATUS_REG0	
0x8	INF_NICAM_STATUS_REG0	
0xC	INF_NICAM_ADD_REG0	
0x10	INF_MONLEVEL_REG0	
0x14	INF_MPX_LEVEL_REG0	
0x18	INF_DC1_REG0	
0x1C	INF_SUBMAGN_REG0	
0x20	INF_NOISELEVEL_REG0	
0x24	INF_SRCSTATUS_REG0	
0x28	DEM_HWCFG_REG0	
0x2C	DEM_CA1_REG0	
0x30	DEM_CA2_REG0	
0x34	DEM_MPXCFG_REG0	
0x38	DEM_FMSUBCFG_REG0	
0x3C	DEM_SWCFG_REG0	
0x40	DEM_OUT_CFG_REG0	
0x44	MAGDET_THR_REG0	
0x48	NMUTE_FMA2_SAP_REG0	
0x4C	NMUTE_MPX_REG0	
0x50	NMUTE_EIAJ_REG0	
0x54	NICAM_CFG_REG0	
0x58	DDEP_CONTROL_REG0	
0x5C	DEM_LEVELADJUST_REG0	
0x60	DEM_ADC_SEL_REG0	
0x64	MPI_CONTROL_REG0	
0x68	INF_REVID_DD_REG0	
0x6C	INF_CPULOAD_REG0	
0x70	INF_OVMADAPT_REG0	
0x74	DDEP_OPTIONS1_REG0	
0x78	DD_OPTIONS2_REG0	

Table 1: DEMDEC_DSP Register Summary *...Continued*

Offset	Name	Description
0x180A8	SND_DD_STATUS00	
0x180B4	SND_DD_T020	
0x180B8	SND_DD_T010	
0x180BC	SND_DD_M000	
0x3FFE0	SND_DD_INT_STATUS0	
0x3FFE4	SND_DD_INT_ENABLE0	
0x3FFE8	SND_DD_INT_CLEAR0	
0x3FFEC	SND_DD_INT_SET0	
0x3FFFC	SND_DD_MOD_ID0	

Table 2: DEMDEC_DSP Registers

Bit	Symbol	Access	Reset Value	Description
Offset 0x4	***INF_MAIN_STATUS_REG0***			
4:0	STDRES	R	0x00	standard detection result (ASD mode), or selected standard in SSS mode 0: V00; failed to find any standard or not supported by device 1: V01; B/G (still searching, SC2 not (yet) found) 10: V02; D/K (still searching, SC2 not (yet) found) 11: V03; M (still searching, no ident or pilot found) 100: V04; B/G A2 101: V05; B/G NICAM 110: V06; D/K A2 (1) 111: V07; D/K A2 (2) 1000: V08; D/K A2 (3) 1001: V09; D/K NICAM 1010: V10; L NICAM 1011: V11; I NICAM 1100: V12; M Korea 1101: V13; M BTSC 1110: V14; M EIAJ 1111: V15; FM Radio, IF = 10.7 MHz, 50 us deemphasis 0x10: V16; FM Radio, IF = 10.7 MHz, 75 us deemphasis 0x11: V17; FM Radio, selectable IF, 50 us deemphasis 0x12: V18; FM Radio, selectable IF, 75 us deemphasis 0x1F: V31; still searching for a standard (can occur a short time after RESTART)
5	GST	R	0x0	general stereo flag (ident source determined by currently detected or selected standard) 0: V0; No stereo mode 1: V1; Stereo mode detected

Table 2: DEMDEC_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
6	GDU	R	0x0	general dual flag 0: V0; No dual mode 1: V1; Dual mode detected
7	APILOT	R	0x0	A2 or EIAJ pilot tone detected 0: V0; False 1: V1; True
8	ADU	R	0x0	A2 or EIAJ ident dual flag 0: V0; False 1: V1; True
9	AST	R	0x0	A2 or EIAJ ident stereo flag 0: V0; False 1: V1; True
10	AAMUT	R	0x0	SC2 (if A2 mode) or EIAJ subchannel muted due to noise 0: V0; False 1: V1; True
11	BPILOT	R	0x0	BTSC or FM radio pilot tone detected (stereo indicator) 0: V0; False 1: V1; True
12	SAPDET	R	0x0	SAP carrier detected 0: V0; False 1: V1; True
13	BAMUT	R	0x0	BTSC stereo or FM Radio muted due to noise 0: V0; False 1: V1; True
14	SAPMUT	R	0x0	SAP muted due to noise 0: V0; False 1: V1; True
15	VDSP_C	R	0x0	NICAM decoder VDSP flag 0: V0; DATA or undefined format 1: V1; SOUND
16	NICST_C	R	0x0	NICAM decoder stereo flag 0: V0; False 1: V1; True
17	NICDU_C	R	0x0	NICAM decoder dual flag 0: V0; False 1: V1; True
18	NAMUT	R	0x0	NICAM automute flag 0: V0; not muted, or no NICAM standard 1: V1; muted (analog sound carrier output)

Table 2: DEMDEC_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
19	RSSF	R	0x0	NICAM reserve sound switching flag (=C4), see NICAM specification 0: V0; analog sound carrier conveys different contents than NICAM carrier 1: V1; analog sound carrier conveys same contents as NICAM carrier (M1 if DUAL)
20	INITSTAT	R	0x0	initialization status (set to 0 after read access) 0: V0; no reset performed since last read 1: V1; reset has been applied to DSP and init routine has been executed
21	SRC_UNLOCK	R	0x0	SRC out of lock flag (output or 32 kHz PLL) 0: V0; SRC in normal operation 1: V1; SRC out of lock, outputs are muted or distorted
23:22	SRD_STATUS	R	0x0	sample rate detector 0: V0; 32 kHz 1: V1; 44.1 kHz 10: V2; 48 kHz 11: V3; less than 6 kHz / invalid I2S input clock
Offset 0x8	***INF_NICAM_STATUS_REG0***			
7:0	ERR_OUT	R	0x00	NICAM error counter: number of parity errors found in the previous 128ms period
8	CFC	R	0x0	NICAM ConFiguration Change 0: V0; No configuration change 1: V1; Configuration change at the 16 frame (CO) boundary
9	CO_LOCKED	R	0x0	NICAM frame and CO synchronization 0: V0; not in sync, NICAM decoder output is muted 1: V1; Decoder has both frame and CO (16 frames) synchronization
13:10	NACB	R	0x0	NICAM application control bits (C1..C4), C4 is also called RSSF and copied to main status register
14	VDSP	R	0x0	identification of NICAM sound 0: V0; DATA or undefined format 1: V1; SOUND
15	NICST	R	0x0	NICAM stereo flag 0: V0; No NICAM stereo mode 1: V1; NICAM stereo mode
16	NICDU	R	0x0	NICAM dual mono mode 0: V0; No NICAM dual mono mode 1: V1; NICAM dual mono mode
23:17	RSD_23To17	R	0x00	reserved
Offset 0xC	***INF_NICAM_ADD_REG0***			
10:0	ADW	R	0x000	additional data word (11 bits per frame, updated every 1 ms)

Table 2: DEMDEC_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
12:11	PARCHK	R	0x0	CI bits, decoded by majority logic from the parity checks of the last ten samples in a frame.
13	SAD	R	0x0	new additional data bits have been received, reset when data are read. 0: V0; False 1: V1; True
14	OVW	R	0x0	new additional data bits have been received, but the previous bits had not been read (overrun flag) 0: V0; False 1: V1; True
23:15	RSD_23To15	R	0x000	reserved
Offset 0x10	***INF_MONLEVEL_REG0***			
23:0	DD_MONLEVEL	R	0x000000	monitor level
Offset 0x14	***INF_MPX_LEVEL_REG0***			
5:0	RSD_5To0	R	0x00	reserved
23:6	MPXPLEVEL	R	0x00000	MPX pilot level
Offset 0x18	***INF_DC1_REG0***			
23:0	SC1_DC	R	0x000000	DC offset of sound carrier 1 after FM demodulation
Offset 0x1C	***INF_SUBMAGN_REG0***			
23:0	SUBMAGN	R	0x000000	magnitude of FM subchannel
Offset 0x20	***INF_NOISELEVEL_REG0***			
0	NDETCH_STAT	R	0x0	status noise detector channel 0: V0; channel 1 1: V1; channel 2
1	NDETPB_STAT	R	0x0	status noise detector passband 0: V0; low (2.5 fh) 1: V1; high (7.5 fh)
23:2	NOISELEVEL	R	0x000000	noise detector output
Offset 0x24	***INF_SRCSTATUS_REG0***			
0	SRCSTAT_FMA2	R	0x0	SRC and preprocessing for FMA2 0: V0; inactive 1: V1; ACTIVE
1	SRCSTAT_FMMONO	R	0x0	SRC and preprocessing for FMMONO 0: V0; inactive 1: V1; ACTIVE
2	SRCSTAT_BTSC	R	0x0	SRC and preprocessing for MPX (BTSC, FMRADIO) 0: V0; inactive 1: V1; ACTIVE
3	RSD_Bit3	R	0x0	reserved

Table 2: DEMDEC_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
4	SRCSTAT_SAP	R	0x0	SRC and preprocessing for SAP 0: V0; inactive 1: V1; ACTIVE
5	SRCSTAT_NICAM	R	0x0	SRC and preprocessing for NICAM 0: V0; inactive 1: V1; ACTIVE
6	SRCSTAT_EXTAM	R	0x0	SRC and preprocessing for EXTAM 0: V0; inactive 1: V1; ACTIVE
7	SRCSTAT_PIPMONO	R	0x0	SRC and preprocessing for PIPMONO 0: V0; inactive 1: V1; ACTIVE
8	SRCSTAT_ADC	R	0x0	SRC and preprocessing for ADC 0: V0; inactive 1: V1; ACTIVE
11:9	SRCSTAT_NUMCH	R	0x0	number of active SRC channels, considering one and two channels paths
13:12	SRCSTAT_THREAD32	R	0x0	PLL state of 32 kHz thread (NICAM) 0: V0; not locked 1: V1; not fully locked, PLL stage 1 11: V3; locked, PLL stage 2
15:14	SRCSTAT_THREAD35	R	0x0	PLL state of 35 kHz thread (analog demodulators) 0: V0; not locked 1: V1; not fully locked, PLL stage 1 11: V3; locked, PLL stage 2
17:16	SRCSTAT_THREAD53	R	0x0	PLL state of 53 kHz thread (ADC inputs) 0: V0; not locked 1: V1; not fully locked, PLL stage 1 11: V3; locked, PLL stage 2
19:18	SRCSTAT_THREADOUT	R	0x0	PLL state of output thread 0: V0; not locked 1: V1; not fully locked, PLL stage 1 11: V3; locked, PLL stage 2
21:20	RSD_21To20	R	0x0	reserved
22	SRCSTAT_UPDWN35	R	0x0	mode of 35 kHz to output SRC 0: V0; down sampling 1: V1; up sampling
23	RSD_Bit23	R	0x0	reserved

Table 2: DEMDEC_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
Offset 0x28	***DEM_HWCFG_REG0***			
1:0	CH2MOD	R/W	0x0	operating mode of demodulator channel 2 0: V0; FM 1: V1; AM 10: V2; NICAM
2	CH1MOD	R/W	0x0	operating mode of demodulator channel 1 0: V0; FM 1: V1; AM
3	INITLPF	R/W	0x0	initialization of loop filters in demodulator 0: V0; normal operation 1: V1; initialization (reset to zero)
4	RSD_Bit4	R/W	0x0	reserved, must be written as 0
6:5	FILTBW_M	R/W	0x0	sound carrier filter bandwidth 0: V0; narrow 1: V1; extra wide (high deviation mode) 10: V2; medium 11: V3; wide
8:7	IDMOD_M	R/W	0x0	FM ident speed 0: V0; slow 1: V1; medium 10: V2; fast 11: V3; off (reset)
10:9	IDAREA	R/W	0x0	Area/regional code for FM identification 0: V0; Europe 1: V1; Korea 10: V2; Japan 11: V3; Japan
11	BPILCAN	R/W	0x0	MPX pilot cancellation 0: V0; off 1: V1; on
12	FM_MPX	R/W	0x0	input from demodulator hardware at 4*fs 0: V0; FM / AM output 1: V1; MPX demodulator output
14:13	ID_DC_LEVEL	R/W	0x0	DC level for IDENT pilot detection 0: V0; Level > 3 1: V1; Level > 4 10: V2; Level > 5 11: V3; Level > 6
15	ID_BYBPF	R/W	0x0	bypass bandpass filter level detector 0: V0; off 1: V1; on

Table 2: DEMDEC_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
16	NOISELEV_EN	R/W	0x0	enable output register noise level BSJ 0: V0; disable 1: V1; enable
17	PILOTLEV_EN	R/W	0x0	enable output register pilot level BSJ 0: V0; disable 1: V1; enable
23:18	RSD_23To18	R/W	0x00	reserved, must be written as 0
Offset 0x2C	***DEM_CA1_REG0***			
23:0	CARRIER1	R/W	0x000000	sound carrier 1 (mixer 1) frequency 0x555555: V555555; 4.5 MHz 0x684BDA: V684BDA; 5.5 MHz 0x71C71C: V71C71C; 6.0 MHz 0x7B425F: V7B425F; 6.5 MHz 0xCAE759: VCAE759; 10.7 MHz
Offset 0x30	***DEM_CA2_REG0***			
23:0	CARRIER2	R/W	0x000000	sound carrier 2 (mixer 2) frequency 0x5994BF: V5994BF; 4.724 MHz 0x6CE2A5: V6CE2A5; 5.742 MHz 0x6EEEEF: V6EEEEF; 5.85 MHz 0x76AB94: V76AB94; 6.258 MHz 0x7C3ECE: V7C3ECE; 6.552 MHz
Offset 0x34	***DEM_MPXCFG_REG0***			
0	RSD_Bit0	R/W	0x0	reserved, must be written as 0
1	MPX_PLL_BW	R/W	0x0	MPX demodulator pilot PLL bandwidth 0: V0; 5Hz (default) 1: V1; 10Hz
23:2	MPX_FREQ	R/W	0x000000	MPX pilot frequency 0x25ED1: V25ED1; 15625 Hz (PAL line freq.) 0x2630C: V2630C; 15734 Hz (NTSC line freq.) 0x2E1E3: V2E1E3; 19000 Hz (FM radio)
Offset 0x38	***DEM_FMSUBCFG_REG0***			
0	FMSUB_BW	R/W	0x0	FM subchannel and EIAJ MAIN filter bandwidth 0: V0; narrow 1: V1; wide
2:1	EIAJ_DELAY	R/W	0x0	delay fine adjustment in MAIN path for EIAJ stereo
3	NDETCH	R/W	0x0	noise detector channel 0: V0; channel 1 1: V1; channel 2
4	NDETPB	R/W	0x0	noise detector passband 0: V0; low (2.5 fh) 1: V1; high (7.5 fh)
7:5	RSD_7To5	R/W	0x0	reserved, must be written as 0

Table 2: DEMDEC_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
23:8	FMSUB_FREQ	R/W	0x0000	FM subchannel frequency (SAP or Japan) 0x1318: V1318; 2 fh for EIAJ 0x2FBD: V2FBD; 5 fh for SAP
Offset 0x3C	***DEM_SWCFG_REG0***			
0	FMMONOBW	R/W	0x0	audio bandwidth for FMMONO path 0: V0; maximum 1: V1; 14 kHz
3:1	BTSCPATH	R/W	0x0	processing in BTSC path 0: V0; BTSC stereo (75 us fixed deemphasis + dbx) 1: V1; FM Radio + fixed deemphasis 10: V2; SAT adaptive deemphasis 11: V3; EIAJ (Japanese M std.) 100: V4; BTSC stereo FLAT (for testing only)
6:4	FMDEEM	R/W	0x0	fixed deemphasis for FMA2, FMMONO, FMRADIO and EIAJ paths 0: V0; 50 us 1: V1; 60 us 10: V2; 75 us 11: V3; J17 100: V4; OFF / flat
8:7	SAPDEEM	R/W	0x0	SAP decompression mode 0: V0; 150 us deemphasis 1: V1; OFF / flat 10: V2; reserved 11: V3; dbx
11:9	RSD_11To9	R/W	0x0	reserved, must be written as 0
12	SRC_FMA2	R/W	0x0	SRC and preprocessing for FMA2 0: V0; inactive 1: V1; ACTIVE
13	SRC_FMMONO	R/W	0x0	SRC and preprocessing for FMMONO 0: V0; inactive 1: V1; ACTIVE
14	SRC_BTSC	R/W	0x0	SRC and preprocessing for BTSC 0: V0; inactive 1: V1; ACTIVE
15	RSD_Bit15	R/W	0x0	reserved, must be written as 0
16	SRC_SAP	R/W	0x0	SRC and preprocessing for SAP 0: V0; inactive 1: V1; ACTIVE
17	SRC_NICAM	R/W	0x0	SRC and preprocessing for NICAM 0: V0; inactive 1: V1; ACTIVE

Table 2: DEMDEC_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
18	SRC_EXTAM	R/W	0x0	SRC and preprocessing for EXTAM 0: V0; inactive 1: V1; ACTIVE
19	SRC_PIPMONO	R/W	0x0	SRC and preprocessing for PIPMONO 0: V0; inactive 1: V1; ACTIVE
20	SRC_ADC	R/W	0x0	SRC and preprocessing for ADC 0: V0; inactive 1: V1; ACTIVE
23:21	RSD_23To21	R/W	0x0	reserved, must be written as 0
Offset 0x40	***DEM_OUT_CFG_REG0***			
2:0	FMDEMAT	R/W	0x0	FM dematrix 0: V0; mono CH1 1: V1; mono CH2 10: V2; dual (transparent, identity matrix) 11: V3; stereo Europe 100: V4; stereo M standards (BTSC, Korea, Japan) or FM Radio
4:3	FM_SCALE	R/W	0x0	scaling of FM signals (FMA2, FMMONO) 0: V0; 27 kHz nominal FM deviation (Europe) 1: V1; 15 kHz nominal FM deviation (M standards) 10: V2; 0 dB gain
5	MUTE_DEC_MONO	R/W	0x1	mute DEC and MONO outputs (expert mode) (softmute) 0: V0; no mute 1: V1; mute
6	MUTE_SAP	R/W	0x1	mute SAP output (expert mode) (softmute) 0: V0; no mute 1: V1; mute
11:7	RSD_11To7	R/W	0x00	reserved, must be written as 0

Table 2: DEMDEC_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
16:12	DD_MON_SRC	R/W	0x00	source for monitor function (also available in DDEP mode) 0: V00; FM,AM,MPX (1 fs) input 1: V01; FM,AM,MPX (4 fs) input 10: V02; FM dematrix input 11: V03; FM dematrix output 100: V04; NICAM 101: V05; FMMONO 110: V06; SAP 111: V07; EXTAM 1000: V08; PIPMONO 1001: V09; ADC 1010: V0A; FM/AM/BTSC DC 1011: V0B; DEC output 1100: V0C; MONO output
18:17	DD_MON_DET	R/W	0x0	detection type for monitor function (also in DDEP mode) 0: V0; random samples 1: V1; absolute value peak detection 10: V2; quasi peak detection 11: V3; off / reset peak detector
20:19	DD_MON_MATRIX	R/W	0x0	matrix for monitor source (also in DDEP mode) 0: V0; A 1: V1; (A+B)/2 (2-ch. sources only) 10: V2; B (2-ch. sources only) 11: V3; (A-B)/2 (2-ch. sources only)
23:21	RSD_23To21	R/W	0x0	reserved, must be written as 0
Offset 0x44	***MAGDET_THR_REG0***			
3:0	MPX_PILOT_THR_UP	R/W	0x4	upper threshold for MPX pilot detection (BTSC, FM RADIO) in dB below nominal level
7:4	MPX_PILOT_THR_LO	R/W	0x8	lower threshold for MPX pilot detection (BTSC, FM RADIO) in dB below nominal level
11:8	SAP_CAR_THR_UP	R/W	0x3	upper threshold for SAP carrier detection in dB below nominal level
15:12	SAP_CAR_THR_LO	R/W	0x6	lower threshold for SAP carrier detection in dB below nominal level
17:16	RSD_17To16	R/W	0x0	reserved, must be written as 0
22:18	ASD_SC1_THR	R/W	0x00	threshold for detection of first sound carrier (SC1) during ASD first step, relative to -30 dBFS. -16 sets threshold=0 to prevent failure.
23	RSD_Bit23	R/W	0x0	reserved, must be written as 0
Offset 0x48	***NMUTE_FMA2_SAP_REG0***			
4:0	NMUTE_SAP_THR	R/W	0x00	noise threshold adjustment for automute of SAP (-16 means automute off)
8:5	NMUTE_SAP_HYST	R/W	0x4	hysteresis size [dB] for automute of SAP

Table 2: DEMDEC_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
13:9	NMUTE_SC2_THR	R/W	0x00	noise threshold adjustment for automute of SC2 in FM A2 standards (-16 means automute off)
17:14	NMUTE_SC2_HYST	R/W	0x4	hysteresis size [dB] for automute of SC2 in FM A2 standards
23:18	RSD_23To18	R/W	0x00	reserved, must be written as 0
Offset 0x4C	***NMUTE_MPX_REG0***			
4:0	NMUTE_BTSC_THR	R/W	0x00	noise threshold adjustment for automute of BTSC stereo carrier (-16 means automute off)
8:5	NMUTE_BTSC_HYST	R/W	0x4	hysteresis size [dB] for automute of BTSC stereo
13:9	NMUTE_FMRA_THR	R/W	0x00	noise threshold adjustment for automute of FM RADIO stereo carrier (-16 means automute off)
17:14	NMUTE_FMRA_HYST	R/W	0x4	hysteresis size [dB] for automute of FM RADIO stereo
23:18	RSD_23To18	R/W	0x00	reserved, must be written as 0
Offset 0x50	***NMUTE_EIAJ_REG0***			
4:0	NMUTE_EIAJ_THR	R/W	0x00	noise threshold adjustment for automute of EIAJ FM subcarrier (-16 means automute off)
8:5	NMUTE_EIAJ_HYST	R/W	0x3	hysteresis size [dB] for automute of EIAJ FM subcarrier
12:9	EIAJ_CAR_THR_UP	R/W	0x8	upper threshold for EIAJ SUB carrier detection in dB below nominal level
16:13	EIAJ_CAR_THR_LO	R/W	0xC	lower threshold for EIAJ SUB carrier detection in dB below nominal level
17	EIAJ_CAR_DETECT	R/W	0x1	enable EIAJ SUB carrier detector 0: V0; sub carrier detector disabled 1: V1; sub carrier detector enabled
23:18	RSD_23To18	R/W	0x00	reserved, must be written as 0
Offset 0x54	***NICAM_CFG_REG0***			
0	ONLY_RELATED	R/W	0x0	reproduce only related NICAM on DEC output (DDEP only) 0: V0; false (NICAM whenever possible) 1: V1; true (NICAM suppressed if RSSF=0)
1	RSD_Bit1	R/W	0x0	reserved, must be written as 0
2	EXTAM	R/W	0x1	NICAM fall back source in case of NICAM L automute (DDEP only) 0: V0; channel 1 AM demodulator output 1: V1; EXTAM (external AM demodulator)
3	NICDEEM	R/W	0x0	deemphasis (J17) for NICAM 0: V0; ON 1: V1; OFF (flat)
4	NIC_AMUTE	R/W	0x0	NICAM auto mute function depending on bit error rate (DDEP only) 0: V0; ON 1: V1; OFF
12:5	NICLOERRLIM	R/W	0x64	NICAM lower bit error limit for automute (DDEP only)
20:13	NICUPERRLIM	R/W	0xC8	NICAM upper bit error limit for automute (DDEP only)

Table 2: DEMDEC_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
21	NICERRDETLO	R/W	0x0	select NICAM bit error detector type for lower threshold 0: V0; hardware, 128 ms fixed 1: V1; software, adjustable time
23:22	RSD_23To22	R/W	0x0	reserved, must be written as 0
Offset 0x58	***DDEP_CONTROL_REG0***			
1:0	EPMODE	R/W	0x0	DEMDEC Easy Programming (DDEP) mode 0: V0; 'AUTO STANDARD DET.' (ASD), STDSEL[4:0] defines the set of detectable standards. 1: V1; 'STATIC STANDARD SELECT' (SSS). STDSEL[4:0] contains standard code. 11: V3; DEMDEC expert mode (fully manual mode, DDEP disabled)
6:2	STDSEL	R/W	0x00	Bits multiplexed for ASD and SSS modes.In ASD mode (EPMODE=0): flags for allowed standards B/G | D/K | L/L' | I | M (LSB to MSB). In SSS mode (EPMODE=1): standard code as defined in status register STDRES, e.g. code 4 selects B/G A2.
7	REST	R/W	0x0	RESTART decoder and initialize Easy Programming after channel switch, if changed from 0 to 1.
8	OVMADAPT	R/W	0x1	FM overmodulation adaptation (avoids distortion, filter bandwidth and gain is chosen adaptively) 0: V0; disabled 1: V1; enabled (recommended)
9	DDMUTE	R/W	0x0	mute DEMDEC output signals 0: V0; not muted 1: V1; muted
11:10	FILTBW	R/W	0x0	sound carrier filter bandwidth (like FILTBW_M). NOT effective if BTSC, EIAJ, FMRADIO active, or if OVMADPT=1 0: V0; narrow (recommended) 1: V1; extra wide 10: V2; medium 11: V3; wide
13:12	IDMOD	R/W	0x0	FM ident speed in SSS mode (otherwise not effective) 0: V0; slow 1: V1; medium 10: V2; fast 11: V3; off (reset)
14	RSD_Bit14	R/W	0x0	reserved, must be written as 0
15	RSD_Bit15	R/W	0x0	reserved, must be written as 0
16	SAPDBX	R/W	0x0	SAP decompression mode 0: V0; dbx used for BTSC stereo decoding, fixed compromise deemphasis for SAP (recommended) 1: V1; dbx used for SAP, BTSC stereo forced to mono

Table 2: DEMDEC_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
17	FHPAL	R/W	0x0	line frequency for BTSC decoding 0: V0; NTSC line frequency (15.734 kHz) used in SSS, or preferred in ASD mode 1: V1; PAL line frequency (15.625 kHz) used in SSS, or preferred in ASD mode
19:18	OVMTHR	R/W	0x1	overmodulation level threshold relative to nominal (applies if OVMADPT=1) 0: V0; +3 dB = -12 dBFS 1: V1; +6 dB = - 9 dBFS (recommended) 10: V2; +9 dB = -6 dBFS 11: V3; +12 dB= -3 dBFS
20	BGA2PREF	R/W	0x0	BG A2 preference selection 0: V0; start with NICAM search 1: V1; start with A2 search, NICAM found only after timeout
21	RSD_Bit21	R/W	0x0	reserved, must be written as 0
23:22	SRCPREF	R/W	0x0	select channels to convert via SRC (see documentation) 0: V0; DECoder, 3. language and ADC (not PIPMONO) 1: V1; DECoder, PIPMONO and ADC (not 3. language) 10: V2; DECoder. PIPMONO and 3. language (not ADC) 11: V3; MONO, PIPMONO, 3. language and ADC (DEC only MONO)
Offset 0x5C	***DEM_LEVELADJUST_REG0***			
4:0	EXTAM_GAIN	R/W	0x00	level adjust (gain) for EXTAM signal from ADC (+15..-15 dB, -16 = MUTE)
9:5	NICAM_GAIN	R/W	0x00	DDEP mode: extra gain for NICAM signal, added to internal gain (+15..-15 dB, -16 = MUTE) In expert mode: internal NICAM scaling
11:10	RSD_11To10	R/W	0x0	reserved, must be written as 0
23:12	ANLG_SCALE	R/W	0x400	expert mode: internal scaling coefficient for all analog demodulator signals. 1024 means 0 dB.
Offset 0x60	***DEM_ADC_SEL_REG0***			
1:0	MAP_EXTAM	R/W	0x0	ADC channel from I2D to EXTAM 0: V0; primary channel 1 1: V1; primary channel 2 10: V2; secondary channel 1 11: V3; secondary channel 2
3:2	MAP_PIPMONO	R/W	0x1	ADC channel from I2D to PIPMONO 0: V0; primary channel 1 1: V1; primary channel 2 10: V2; secondary channel 1 11: V3; secondary channel 2

Table 2: DEMDEC_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
5:4	MAP_ADCST_L	R/W	0x2	ADC channel from I2D to ADC stereo ch. L 0: V0; primary channel 1 1: V1; primary channel 2 10: V2; secondary channel 1 11: V3; secondary channel 2
7:6	MAP_ADCST_R	R/W	0x3	ADC channel from I2D to ADC stereo ch. R 0: V0; primary channel 1 1: V1; primary channel 2 10: V2; secondary channel 1 11: V3; secondary channel 2
8	MUTE_PIPMONO	R/W	0x1	soft mute PIPMONO channel 0: V0; not muted 1: V1; muted
9	MUTE_ADCST_LR	R/W	0x1	soft mute both ADC channels 0: V0; not muted 1: V1; muted
23:10	RSD_23To10	R/W	0x0000	reserved, must be written as 0
Offset 0x64	***MPI_CONTROL_REG0***			
7:0	MPIDIV	R/W	0x01	MPI rate divider, MPI rate = 53 kHz / MPIDIV. If 0, selects highest possible MPI rate (DD-DSP: 53 kHz)
23:8	RSD_23To8	R/W	0x0000	reserved, must be written as 0
Offset 0x68	***INF_REVID_DD_REG0***			
3:0	MAJOR_VERSION_NR_DD	R	0x0	major version number
7:4	MINOR_VERSION_NR_DD	R	0x0	minor version number
11:8	PATCH_LEVEL_DD	R	0x0	patch level number. incremented number indicates bugfixes of the embedded software without any change of control interface or functionality. no driver update needed.
15:12	DEVICE_TYPE_DD	R	0x0	device type and hardware version expected by DSP software 0: V0; PNX2000 N1 1: V1; PNX2000 N2 10: V2; PNX2000 N3 100: V4; PNX2000 N1 101: V5; PNX2000 N2
23:16	RSD_23To16	R	0x00	reserved
Offset 0x6C	***INF_CPULOAD_REG0***			
23:0	DD_CPULOAD	R	0x000000	CPU load indicator; ratio of busy time to waiting time averaged over approx. 2^24 clock cycles.

Table 2: DEMDEC_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
Offset 0x70	***INF_OVMADAPT_REG0***			
1:0	FILTBW_STAT	R	0x0	indicates internal FM/AM filter bandwidth (FILTBW) 0: V0; narrow 1: V1; extra wide 10: V2; medium 11: V3; wide
11:2	RSD_11To2	R	0x000	reserved
23:12	OVM_SCALE_STAT	R	0x000	current scaling factor for OVMADAPT (off: 1024 = 0 dB)
Offset 0x74	***DDEP_OPTIONS1_REG0***			
2:0	SRC_CFG_TABLE	R/W	0x0	SRC configuration table 0: V0; 5 channels max. 1: V1; 6 channels max. 10: V2; 4 channels max. 11: V3; 3 channels max., no PIPMONO and ADC 100: V4; table in YRAM (default identical with 5 channel table)
3	RSD_Bit3	R/W	0x0	reserved, must be written as 0
5:4	IDMOD_SLOW_EUR	R/W	0x0	in ASD mode, IDMOD setting when European A2 standards (B/G, D/K) are detected 0: V0; slow 1: V1; medium 10: V2; fast
7:6	IDMOD_SLOW_KOR	R/W	0x0	in ASD mode, IDMOD setting when M Korea standard detected 0: V0; slow 1: V1; medium 10: V2; fast
9:8	IDMOD_SLOW_JAP	R/W	0x1	in ASD mode, IDMOD setting when EIAJ standard detected 0: V0; slow 1: V1; medium 10: V2; fast
10	NICAMCPLL_ACQHELP_OFF	R/W	0x0	acquisition help for NICAM carrier loop 0: V0; active 1: V1; disabled
18:11	NICAM_ERRDETECTTIME	R/W	0x08	detection time interval for software bit error detector, in multiples of 32 ms
19	SAP_BW	R/W	0x0	SAP filter bandwidth selection 0: V0; narrow filter 1: V1; wide filter
23:20	RSD_23To20	R/W	0x0	reserved, must be written as 0

Table 2: DEMDEC_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
Offset 0x78	***DD_OPTIONS2_REG0***			
0	WATCHOUTCLK_OFF	R/W	0x0	watchdog for failure of output audio clock 0: V0; active 1: V1; disabled
1	SRCPLL_OUT_INIT	R/W	0x0	initialize SRC PLL for output thread 0: V0; no action 1: V1; enforce initialization
2	SRCPLL_32K_INIT	R/W	0x0	initialize SRC PLL for 32 kHz input thread 0: V0; no action 1: V1; enforce initialization
3	SRCPLL_35K_INIT	R/W	0x0	initialize SRC PLL for 35 kHz input thread 0: V0; no action 1: V1; enforce initialization
4	SRCPLL_53K_INIT	R/W	0x0	initialize SRC PLL for 53 kHz input thread 0: V0; no action 1: V1; enforce initialization
5	CHECK_SRC_BUFFERS	R/W	0x0	sanity check of SRC buffers, enable only for short time after power up or audio clock interruption 0: V0; disabled 1: V1; active
23:6	RSD_23To6	R/W	0x00000	reserved, must be written as 0
Offset 0x180A8	***SND_DD_STATUS00***			
23:0	See_INF_MAIN_STATUS_REG	R	0x000000	copy of INF_MAIN_STATUS_REG, suitable for fast access
31:24	RSD_31To24	R	0x00	not used
Offset 0x180B4	***SND_DD_T020***			
14:0	RSD_14To0	R	0x0000	reserved
22:15	EIR_BUS_H	R/W	0x00	EIR_BUS[31:24] Goto mode input for Epics7. See description of the TCB_GOTO_MODE bit in this table.
23	TCB_GOTO_MODE	R/W	0x0	Enable bit for goto mode. The goto mode is a mode in which an instruction can be forced onto the Epics7 instruction bus. The instruction is stored in a register in the Test Control Block (TCB) and is usually a goto instruction to force the DSP to jump to a certain routine in program memory which will never be accessed in functional mode. These routines can be used as test/evaluation routines.
31:24	RSD_31To24	R	0x00	not used
Offset 0x180B8	***SND_DD_T010***			
23:0	EIR_BUS_L	R/W	0x000000	EIR_BUS[23:0] Goto mode input for Epics7. See description of the TCB_GOTO_MODE bit in this table.
31:24	RSD_31To24	R	0x00	not used

Table 2: DEMDEC_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
Offset 0x180BC	***SND_DD_M000***			
0	BIOPRASEL	R/W	0x0	BIOS / program RAM select 0: V0; program RAM 1: V1; BIOS
1	PRAPROSEL	R/W	0x0	program RAM / ROM select 0: V0; program ROM select 1: V1; program RAM select
2	PC_RESET_MPI	R/W	0x0	program counter reset for DEMDEC DSP 0: V0; no reset 1: V1; reset
3	IIC_INT	R/W	0x0	EMMI flag to inform EPICS to interrupt normal processing (mechanism is not used in current version) $0 = no set $1 = set 0: V0; no set 1: V1; set
4	BAM_EN	R/W	0x0	bus allocation minimizer enable 0: V0; disabled 1: V1; enabled
5	DCCANCEL	R/W	0x0	DC cancellation filter enable 0: V0; disabled 1: V1; enabled
23:6	RSD_23To6	R/W	0x00000	reserved
31:24	RSD_31To24	R	0x00	not used
Offset 0x3FFE0	***SND_DD_INT_STATUS0***			
0	STDRES	R	0x0	indicates a pending interrupt condition caused by a change in the standard detection result 0: V0; not pending 1: V1; pending
1	GST	R	0x0	indicates a pending interrupt condition caused by a change in the general stereo flag 0: V0; not pending 1: V1; pending
2	GDU	R	0x0	indicates a pending interrupt condition caused by a change in the general dual flag 0: V0; not pending 1: V1; pending
3	APILOT	R	0x0	indicates a pending interrupt condition caused by a change in the A2 or EIAJ pilot tone flag 0: V0; not pending 1: V1; pending

Table 2: DEMDEC_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
4	ADU	R	0x0	indicates a pending interrupt condition caused a change in the A2 or EIAJ ident dual flag 0: V0; not pending 1: V1; pending
5	AST	R	0x0	indicates a pending interrupt condition caused a change in the A2 or EIAJ ident stereo flag 0: V0; not pending 1: V1; pending
6	AAMUT	R	0x0	indicates a pending interrupt condition caused a change in the SC2 (if A2 mode) or EIAJ subchannel muted due to noise flag 0: V0; not pending 1: V1; pending
7	BPILOT	R	0x0	indicates a pending interrupt condition caused a change in the BTSC or FM radio pilot tone flag (stereo indicator) 0: V0; not pending 1: V1; pending
8	SAPDET	R	0x0	indicates a pending interrupt condition caused a change in the SAP carrier flag 0: V0; not pending 1: V1; pending
9	BAMUT	R	0x0	indicates a pending interrupt condition caused a change in the BTSC stereo muted due to noise flag (if noise detector enabled) 0: V0; not pending 1: V1; pending
10	SAMUT	R	0x0	indicates a pending interrupt condition caused a change in the SAP muted due to noise flag (if noise detector enabled) 0: V0; not pending 1: V1; pending
11	VDSP_C	R	0x0	indicates a pending interrupt condition caused a change in the NICAM decoder VDSP flag 0: V0; not pending 1: V1; pending
12	NICST_C	R	0x0	indicates a pending interrupt condition caused a change in the NICAM decoder stereo flag 0: V0; not pending 1: V1; pending
13	NICDU_C	R	0x0	indicates a pending interrupt condition caused a change in the NICAM decoder dual flag 0: V0; not pending 1: V1; pending

Table 2: DEMDEC_DSP Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
14	NAMUT	R	0x0	indicates a pending interrupt condition caused a change in the NICAM automute flag 0: V0; not pending 1: V1; pending
15	INITSTAT	R	0x0	indicates a pending interrupt condition caused a change in the initialization status (set to 0 upon read access) 0: V0; not pending 1: V1; pending
16	SRC_UNLOCK	R	0x0	indicates a pending interrupt condition caused a change in the SRC out of lock flag 0: V0; not pending 1: V1; pending
23:17	RSD_23To17	R	0x00	reserved
24	TNSACT_GRANT	R	0x0	indicates a pending interrupt caused to inform the DTL initiator that a new transactions on a high latency software control register will be granted (alias: RTF = Ready for Transfer Flag) 0: V0; not pending 1: V1; pending
31:25	RSD_31To25	R	0x00	not used
Offset 0x3FFE4	***SND_DD_INT_ENABLE0***			
24:0	EN_INT_COND	R/W	0x0000000	enable interrupt request condition INT_COND[i] 0: V0; disabled 1: V1; enabled
31:25	RSD_31To25	R	0x00	not used
Offset 0x3FFE8	***SND_DD_INT_CLEAR0***			
24:0	CLR_INT_COND	W	0x0000000	clear interrupt request condition SND_DD_INT_STATUS[i] 0: V0; preserve old state 1: V1; clear
31:25	RSD_31To25	W	0x00	not used
Offset 0x3FFEC	***SND_DD_INT_SET0***			
24:0	SET_INT_COND	W	0x0000000	set interrupt request condition SND_DD_INT_STATUS[i], for debug purposes 0: V0; preserve old state 1: V1; set
31:25	RSD_31To25	W	0x00	not used
Offset 0x3FFFC	***SND_DD_MOD_ID0***			
7:0	APERTURE	R	0x3F	index for aperture size in global memory map (= aperture_size/4K -1)
11:8	MINOR_REV	R	0x0	Minor revision sound core
15:12	MAJOR_REV	R	0x0	Major revision sound core
31:16	ID	R	0xA067	Module identifier sound core

Chapter 5: GPR Registers

PNX2000

Rev. 01 — 15 December 2003

1. GPR Register Descriptions

Table 1: GPR Register Summary

Offset	Name	Description
0x0	GP_CLKEN	Clock Enables <raw_Reset By value="pi_reset_hrd_n"/> <raw_Register No value="1"/>
0x4	GP_CLKSEL	Clock Frequency Selects <raw_Reset By value="pi_reset_hrd_n"/> <raw_Register No value="2"/>
0xC	GP_DISTRICONTROL	Clock Distribution Control bits <raw_Reset By value="pi_reset_hrd_n"/> <raw_Register No value="3"/>
0x10	GP_WSPLLMASTERSEL	WS PLL n, m, and p divide values in master Mode. <raw_Reset By value="pi_reset_hrd_n"/> <raw_Register No value="4"/>
0x14	GP_WSPLLSLAVESEL	WS PLL Control for in uC slave mode. <raw_Reset By value="pi_reset_hrd_n"/> <raw_Register No value="5"/>
0x18	GP_WSPLLCONTROL	WS PLL Mode control. <raw_Reset By value="pi_reset_hrd_n"/> <raw_Register No value="6"/>
0x1C	GP_WSPLLSTATUS	WS PLL Status Register. <raw_Reset By value="(read only)"/> <raw_Register No value="7"/ >
0x20	GP_WS_FSCOUNTER	Counter to determine WS PLL divider ratio in slave mode. <raw_Reset By value="(read only)"/> <raw_Register No value="8"/>
0x24	GP_WS_SAMPLERATE	Sample rate. <raw_Reset By value="(read only)"/> <raw_Register No value="9"/>
0x28	GP_TURBOPLLSEL	TURBO PLL n, m, and p divide values. <raw_Reset By value="pi_reset_hrd_n"/> <raw_Register No value="10"/>
0x2C	GP_TURBOPLLCONTROL	TURBO PLL Control. <raw_Reset By value="pi_reset_hrd_n"/> <raw_Register No value="11"/>
0x30	GP_TURBOPLLSTATUS	TURBO PLL Status Register. <raw_Reset By value="(read only)"/> <raw_Register No value="12"/>

Table 1: GPR Register Summary *...Continued*

Offset	Name	Description
0x34	GP_SYSPLLSEL	SYS PLL n, m, and p divide values. <raw_Reset By value="pi_reset_hrd_n"/> <raw_Register No value="13"/>
0x38	GP_SYSPLLCONTROL	SYS PLL Control. <raw_Reset By value="pi_reset_hrd_n"/> <raw_Register No value="14"/>
0x3C	GP_SYSPLLSTATUS	SYS PLL Status Register. <raw_Reset By value="(read only)"/> <raw_Register No value="15"/>
0x40	GP_LLPLLSEL	SYS PLL n, m, and p divide values. <raw_Reset By value="pi_reset_hrd_n"/> <raw_Register No value="16"/>
0x44	GP_LLPLLCONTROL	LL PLL Control. <raw_Register No value="17"/>
0x48	GP_LLPLLSTATUS	LL PLL Status Register. <raw_Reset By value="(read only)"/> <raw_Register No value="18"/>
0x4C	GP_WSSLAVEPLLCONTROL	WSS Slave PLL control <raw_Reset By value="pi_reset_hrd_n"/> <raw_Register No value="19"/>
0x50	GP_NCOUNTVAL	LL PLL COUNTER VALUE <raw_Reset By value="pi_reset_hrd_n"/> <raw_Register No value="20"/>
0x54	RFU_22	Reserved Register <raw_Reset By value="(read only)"/> <raw_Register No value="21"/>
0x58	GP_RESETS	Controls the resets within the Control Core <raw_Reset By value="pi_reset_n"/> <raw_Register No value="22"/>
0x5C	RFU_28	Reserved Resgister <raw_Reset By value="pi_reset_hrd_n"/> <raw_Register No value="23"/>
0x60	GP_TIMEBASE_1	Time Base VCR PLL control <raw_Register No value="24"/>
0x64	GP_TIMEBASE_2	Time Base VCR PLL status <raw_Register No value="25"/>
0x80	GP_DTM_M_STAB	LOW LATENCY REGISTER IN DTL MMIO CTRL <raw_Register No value="26"/>
0x84	GP_MTD_M_STAB	LOW LATENCY REGISTER IN DTL MMIO CTRL <raw_Register No value="27"/>
0xF00	GP_VCBCONTROL	Version Control Overruling <raw_Reset By value="pi_reset_hrd_n"/> <raw_Register No value="28"/>
0xF04	GP_VCBFUNCTIONS_L	Version Control Debug Functions (lower 32 bits) <raw_Reset By value="pi_reset_hrd_n"/> <raw_Register No value="29"/>
0xF08	GP_VCBFUNCTIONS_H	Version Control Debug Functions (upper 9 bits) <raw_Reset By value="pi_reset_n"/> <raw_Register No value="30"/>

Table 1: GPR Register Summary *...Continued*

Offset	Name	Description
0xF0C	GP_VCBVERSION_OUT	VCB Selected Version <raw_Reset By value="(read only)"/> <raw_Register No value="31"/>
0xF10	GP_VCBFUNC_OUT_L	VCB Function Enable Outputs (lower 32 bits) <raw_Reset By value="(read only)"/> <raw_Register No value="32"/>
0xF14	GP_VCBFUNC_OUT_H	VCB Function Enable Outputs (upper 9 bits) <raw_Reset By value="(read only)"/> <raw_Register No value="33"/>
0xFCC	GP_DEBUGCFG	Debug Configuration Register <raw_Reset By value="pi_reset_n"/> <raw_Register No value="36"/>
0xFE0	GP_IRQ_STAT	<raw_Register No value="34"/>
0xFE4	GP_IRQ_ENAB	LOW LATENCY REGISTER IN DTL MMIO CTRL <raw_Register No value="35"/>
0xFE8	GP_IRQ_CLR	LOW LATENCY REGISTER IN DTL MMIO CTRL
0xFEC	GP_IRQ_SET	LOW LATENCY REGISTER IN DTL MMIO CTRL
0xFFC	GP_MODULE_ID	Module identity of GPRU <raw_Reset By value="(read only)"/> <raw_Register No value="37"/>

Table 2: GPR Registers

Bit	Symbol	Access	Reset Value	Description
Offset 0x0	***GP_CLKEN***			
31:9	RSD_31To9	R	0x000000	non-existent bits. Reads zero <raw_Lowest Bit value="9"/>
8	GP_MPIFCLKEN	R/W	0x0	Clock enable '0' off, '1' on <raw_Lowest Bit value="8"/>
7	GP_DCUCLKEN	R/W	0x0	Clock enable '0' off, '1' on <raw_Lowest Bit value="7"/>
6	GP_DCURXCLKEN	R/W	0x0	Clock enable '0' off, '1' on <raw_Lowest Bit value="6"/>
5	GP_ITU_CLKEN	R/W	0x0	Clock enable '0' off, '1' on <raw_Lowest Bit value="5"/>
4	GP_I2DCLKEN	R/W	0x0	Clock enable '0' off, '1' on <raw_Lowest Bit value="4"/>
3	GP_VIDDECCLK54_1EN	R/W	0x0	Clock enable '0' off, '1' on <raw_Lowest Bit value="3"/>
2	GP_DECI6P75CLKEN	R/W	0x0	Clock enable '0' off, '1' on <raw_Lowest Bit value="2"/>
1	GP_DEMDEC13P5CLKEN	R/W	0x0	Clock enable '0' off, '1' on <raw_Lowest Bit value="1"/>
0	GP_DEMDEC27CLKEN	R/W	0x0	Clock enable '0' off, '1' on <raw_Lowest Bit value="0"/>
Offset 0x4	***GP_CLKSEL***			
31:7	RSD_31To7	R	0x0000000	non-existent bits. Reads zero <raw_Lowest Bit value="7"/>
6	GP_LLPLLREFCLKSEL	R/W	0x0	0':hsync, '1':xtal <raw_Lowest Bit value="6"/>
5	GP_ADACCLKSEL	R/W	0x0	0':128*fs, '1':256*fs <raw_Lowest Bit value="5"/>
4	GP_MPIFCLKSEL	R/W	0x0	'0':13.5MHz, '1':27MHz <raw_Lowest Bit value="4"/>
3:2	GP_ITUCLKSEL	R/W	0x0	00: 64.8 MHz, 01: 32.4 MHz, 10: Line locked PLL, 11 line locked external input <raw_Lowest Bit value="2"/>

Table 2: GPR Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
1	GP_DTOFREQSEL_VID	R/W	0x0	'0': 27 MHz, '1' 54 MHz <raw_Lowest Bit value="1"/>
0	GP_XTALCLKSEL	R/W	0x0	0' x_in, '1' x_in/2 <raw_Lowest Bit value="0"/>
Offset 0xC	***GP_DISTRICONTROL***			
31:8	RSD_31To8	R	0x000000	non-existent bits. Reads zero <raw_Lowest Bit value="8"/>
7	GP_SOFTRESETEPICS	R/W	0x0	Active high soft reset (min. two 6.75 MHz periods) <raw_Lowest Bit value="7"/>
6	GP_SOFTRESET128FS	R/W	0x0	Active high soft reset 128fs (min. two 6.75 MHz periods) <raw_Lowest Bit value="6"/>
5	GP_ADAC_CLKEN	R/W	0x0	<raw_Lowest Bit value="5"/>
4	GP_HALF_MCH	R/W	0x0	HALF_MCH (0: Full MCH speed; 1: Half MCH speed) <raw_Lowest Bit value="4"/>
3	GP_INV128FSA	R/W	0x0	'1' Inverts CLK128FSA <raw_Lowest Bit value="3"/>
2	GP_ENBCLK	R/W	0x0	'1' Enable for local bitclock <raw_Lowest Bit value="2"/>
1	GP_EN128FS	R/W	0x0	'1' Enable for CLK128FSD & CLK128FSA <raw_Lowest Bit value="1"/>
0	GP_ENEP	R/W	0x0	'1' Enable for CLKEP2 <raw_Lowest Bit value="0"/>
Offset 0x10	***GP_WSPLLMASTERSEL***			
31:30	RSD_31To30	R	0x0	non-existent bits. Reads zero <raw_Lowest Bit value="30"/>
29:26	GP_SELR	R/W	0x0	Pins to select bandwidth <raw_Lowest Bit value="26"/>
25:22	GP_SELI	R/W	0x2	Pins to select bandwidth <raw_Lowest Bit value="22"/>
21:17	GP_SELP	R/W	0x1F	Pins to select bandwidth <raw_Lowest Bit value="17"/>
16:0	GP_MDEC	R/W	0x05B69	m: Feedback divider <raw_Lowest Bit value="0"/>
Offset 0x14	***GP_WSPLLSLAVESEL***			
31:30	RSD_31To30	R	0x0	non-existent bits. Reads zero <raw_Lowest Bit value="30"/>
29:26	GP_WSSELR	R/W	0x0	Pins to select bandwidth <raw_Lowest Bit value="26"/>
25:22	GP_WSSELI	R/W	0x4	Pins to select bandwidth <raw_Lowest Bit value="22"/>
21:17	GP_WSSELP	R/W	0x1F	Pins to select bandwidth <raw_Lowest Bit value="17"/>
16:0	GP_WSMDEC	R/W	0x0002D	m: Feedback divider <raw_Lowest Bit value="0"/>
Offset 0x18	***GP_WSPLLCONTROL***			
31:27	RSD_31To27	R	0x00	non-existent bits. Reads zero <raw_Lowest Bit value="27"/>
26	GP_TESTMODEENABLE	R/W	0x0	Enables a testmode for testing the WS PLL with low frequencies <raw_Lowest Bit value="26"/>
25	GP_SLAVETYPE	R/W	0x0	'0' Slave uC mode. '1' Slave auto mode (ignored if master mode is active) <raw_Lowest Bit value="25"/>
24	GP_AUTOMASTERENABLE	R/W	0x0	1 enables automatic change between master/slave mode <raw_Lowest Bit value="24"/>
23	GP_MASTERENABLE	R/W	0x1	1: Master mode; 0: slave mode (ignored if bit 18 is enabled) <raw_Lowest Bit value="23"/>
22	GP_BYPASS256FS	R/W	0x0	Bypass incoming 256fs SYSCLKIN (0: PLL; 1: Bypass) <raw_Lowest Bit value="22"/>
21	GP_BYPASS512FS	R/W	0x0	Bypass incoming 512fs SYSCLKIN (0: PLL; 1: Bypass) <raw_Lowest Bit value="21"/>

Table 2: GPR Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
20:11	GP_NDEC	R/W	0x029	n: Pre-divider <raw_Lowest Bit value="11"/>
10:4	GP_PDEC	R/W	0x1D	p: Post divider <raw_Lowest Bit value="4"/>
3	GP_WSPLLDIRECTI	R/W	0x0	Directi pin, 1: bypass of pre-divider <raw_Lowest Bit value="3"/>
2	GP_WSPLLDIRECTO	R/W	0x0	Directo pin, 1: bypass of post-divider <raw_Lowest Bit value="2"/>
1	GP_WSPLLBYPASS	R/W	0x0	Bypass pin <raw_Lowest Bit value="1"/>
0	GP_WSPLLPD	R/W	0x1	pd pin <raw_Lowest Bit value="0"/>
Offset 0x1C	***GP_WSPLLSTATUS***			
31:5	RSD_31To5	R	0x0000000	non-existent bits. Reads zero <raw_Lowest Bit value="5"/>
4	GP_WSPLLFR	R	0x0	fr (freeRunning) status (active high) <raw_Lowest Bit value="4"/>
3	GP_WSPLLLOCK	R	0x0	lock status (active high) <raw_Lowest Bit value="3"/>
2	GP_WSPLLNACK	R	0x0	nack pre divide acknowledge status (actiev high) <raw_Lowest Bit value="2"/>
1	GP_WSPLLMACK	R	0x0	mack feedback divide acknowledge status (active high) <raw_Lowest Bit value="1"/>
0	GP_WSPLLPACK	R	0x0	pack post divide acknowledge status (active high) <raw_Lowest Bit value="0"/>
Offset 0x20	***GP_WS_FSCOUNTER***			
31:9	RSD_31To9	R	0x000000	non-existent bits. Reads zero <raw_Lowest Bit value="9"/>
8:0	GP_WSPLLFSCOUNT	R	0x000	Counter to determine WSPLL divider ratio in slave mode <raw_Lowest Bit value="0"/>
Offset 0x24	***GP_WS_SAMPLERATE***			
31:2	RSD_31To2	R	0x00000000	non-existent bits. Reads zero <raw_Lowest Bit value="2"/>
1:0	GP_SAMPLERATE	R	0x0	00: 32kHz, 01: 44kHz, 10:48kHz, 11: Over/underflow <raw_Lowest Bit value="0"/>
Offset 0x28	***GP_TURBOPLLSEL***			
31:30	RSD_31To30	R	0x0	non-existent bits. Reads zero <raw_Lowest Bit value="30"/>
29:26	GP_TURBOSELR	R/W	0x0	Pins to select bandwidth <raw_Lowest Bit value="26"/>
25:22	GP_TURBOSELI	R/W	0xD	Pins to select bandwidth <raw_Lowest Bit value="22"/>
21:17	GP_TURBOSELP	R/W	0x1F	Pins to select bandwidth <raw_Lowest Bit value="17"/>
16:0	GP_TURBOMDEC	R/W	0x01006	m: Feedback divider <raw_Lowest Bit value="0"/>
Offset 0x2C	***GP_TURBOPLLCONTROL***			
31:21	RSD_31To21	R	0x000	non-existent bits. Reads zero <raw_Lowest Bit value="21"/>
20:11	GP_TURBONDEC	R/W	0x002	n: Pre-divider <raw_Lowest Bit value="11"/>
10:4	GP_TURBOPDEC	R/W	0x42	p: Post divider <raw_Lowest Bit value="4"/>
3	GP_TURBOPLLDIRECTI	R/W	0x0	TURBOPLL directi pin. 1: bypass of pre-divider <raw_Lowest Bit value="3"/>
2	GP_TURBOPLLDIRECTO	R/W	0x0	TURBOPLL directo pin. 1: bypass of post-divider <raw_Lowest Bit value="2"/>

Table 2: GPR Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
1	GP_TURBOPLLBYPASS	R/W	0x0	TURBOPLL bypass pin <raw_Lowest Bit value="1"/>
0	GP_TURBOPLLPD	R/W	0x1	TURBOPLL pd pin <raw_Lowest Bit value="0"/>
Offset 0x30	***GP_TURBOPLLSTATUS***			
31:5	RSD_31To5	R	0x0000000	non-existent bits. Reads zero <raw_Lowest Bit value="5"/>
4	GP_TUBOPLLFR	R	0x0	fr (freeRunning) status (active high) <raw_Lowest Bit value="4"/>
3	GP_TURBOPLLLOCK	R	0x0	lock status (active high) <raw_Lowest Bit value="3"/>
2	GP_TURBOPLLNACK	R	0x0	nack pre divide acknowledge status (active high) <raw_Lowest Bit value="2"/>
1	GP_TURBOPLLMACK	R	0x0	mack feedback divide acknowledge status (active high) <raw_Lowest Bit value="1"/>
0	GP_TURBOPLLPACK	R	0x0	pack post divide acknowledge status (active high) <raw_Lowest Bit value="0"/>
Offset 0x34	***GP_SYSPLLSEL***			
31:30	RSD_31To30	R	0x0	non-existent bits. Reads zero <raw_Lowest Bit value="30"/>
29:26	GP_SYSSELR	R/W	0x0	Pins to select bandwidth <raw_Lowest Bit value="26"/>
25:22	GP_SYSSELI	R/W	0x4	Pins to select bandwidth <raw_Lowest Bit value="22"/>
21:17	GP_SYSSELP	R/W	0x07	Pins to select bandwidth <raw_Lowest Bit value="17"/>
16:0	GP_SYSMDEC	R/W	0x00200	m: Feedback divider <raw_Lowest Bit value="0"/>
Offset 0x38	***GP_SYSPLLCONTROL***			
31:21	RSD_31To21	R	0x000	non-existent bits. Reads zero <raw_Lowest Bit value="21"/>
20:11	GP_SYSNDEC	R/W	0x302	n: Pre-divider <raw_Lowest Bit value="11"/>
10:4	GP_SYSPDEC	R/W	0x62	p: Post divider <raw_Lowest Bit value="4"/>
3	GP_SYSPLLDIRECTI	R/W	0x1	SYSPLL directi pin. 1: bypass of pre-divider <raw_Lowest Bit value="3"/>
2	GP_SYSPLLDIRECTO	R/W	0x1	SYSPLL directo pin. 1: bypass of post-divider <raw_Lowest Bit value="2"/>
1	GP_SYSPLLBYPASS	R/W	0x0	SYSPLL bypass pin <raw_Lowest Bit value="1"/>
0	GP_SYSPLLPD	R/W	0x1	SYSPLL pd pin <raw_Lowest Bit value="0"/>
Offset 0x3C	***GP_SYSPLLSTATUS***			
31:5	RSD_31To5	R	0x0000000	non-existent bits. Reads zero <raw_Lowest Bit value="5"/>
4	GP_SYSPLLFR	R	0x0	fr (freeRunning) status (active high) <raw_Lowest Bit value="4"/>
3	GP_SYSPLLLOCK	R	0x0	lock status (active high) <raw_Lowest Bit value="3"/>
2	GP_SYSPLLNACK	R	0x0	nack pre divide acknowledge status (actiev high) <raw_Lowest Bit value="2"/>
1	GP_SYSPLLMACK	R	0x0	mack feedback divide acknowledge status (active high) <raw_Lowest Bit value="1"/>
0	GP_SYSPLLPACK	R	0x0	pack post divide acknowledge status (active high) <raw_Lowest Bit value="0"/>

Table 2: GPR Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
Offset 0x40	***GP_LLPLLSEL***			
31:30	RSD_31To30	R	0x0	non-existent bits. Reads zero <raw_Lowest Bit value="30"/>
29:26	GP_LLSELR	R/W	0x0	Pins to select bandwidth <raw_Lowest Bit value="26"/>
25:22	GP_LLSELI	R/W	0x1	Pins to select bandwidth <raw_Lowest Bit value="22"/>
21:17	GP_LLSELP	R/W	0x1F	Pins to select bandwidth <raw_Lowest Bit value="17"/>
16:0	GP_LLMDEC	R/W	0x02FAE	m: Feedback divider <raw_Lowest Bit value="0"/>
Offset 0x44	***GP_LLPLLCONTROL***			
31:21	RSD_31To21	R	0x000	non-existent bits. Reads zero <raw_Lowest Bit value="21"/>
20:11	GP_LLNDEC	R/W	0x302	n: Pre-divider <raw_Lowest Bit value="11"/>
10:4	GP_LLPDEC	R/W	0x0A	p: Post divider <raw_Lowest Bit value="4"/>
3	GP_LLPLLDIRECTI	R/W	0x1	SYSPLL directi pin. 1: bypass of pre-divider <raw_Lowest Bit value="3"/>
2	GP_LLPLLDIRECTO	R/W	0x0	SYSPLL directo pin. 1: bypass of post-divider <raw_Lowest Bit value="2"/>
1	GP_LLPLLBYPASS	R/W	0x0	SYSPLL bypass pin <raw_Lowest Bit value="1"/>
0	GP_LLPLLPD	R/W	0x1	SYSPLL pd pin <raw_Lowest Bit value="0"/>
Offset 0x48	***GP_LLPLLSTATUS***			
31:5	RSD_31To5	R	0x0000000	non-existent bits. Reads zero <raw_Lowest Bit value="5"/>
4	GP_LLPLLFR	R	0x0	fr (freeRunning) status (active high) <raw_Lowest Bit value="4"/>
3	GP_LLPLLLOCK	R	0x0	lock status (active high) <raw_Lowest Bit value="3"/>
2	GP_LLPLLNACK	R	0x0	nack pre divide acknowledge status (actiev high) <raw_Lowest Bit value="2"/>
1	GP_LLPLLMACK	R	0x0	mack feedback divide acknowledge status (active high) <raw_Lowest Bit value="1"/>
0	GP_LLPLLPACK	R	0x0	pack post divide acknowledge status (active high) <raw_Lowest Bit value="0"/>
Offset 0x4C	***GP_WSSLAVEPLLCONTROL***			
31:17	RSD_31To17	R	0x0000	non-existent bits. Reads zero <raw_Lowest Bit value="17"/>
16:7	GP_WSNDEC	R/W	0x002	n: Pre-divider <raw_Lowest Bit value="7"/>
6:0	GP_WSPDEC	R/W	0x17	p: Post divider <raw_Lowest Bit value="0"/>
Offset 0x50	***GP_NCOUNTVAL***			
31:13	RSD_31To13	R	0x00000	<raw_Lowest Bit value="13"/>
12	GP_1FH_CNT_EN	R/W	0x0	<raw_Lowest Bit value="12"/>
11:0	GP_CNT_VAL	R/W	0x000	<raw_Lowest Bit value="0"/>
Offset 0x54	***RFU_22***			
31:5	RSD_31To5	R	0x0000000	non-existent bits. Reads zero <raw_Lowest Bit value="5"/>
4	RFU_E	R	0x0	fr (freeRunning) status (active high) <raw_Lowest Bit value="4"/>
3	RFU_D	R	0x0	lock status (active high) <raw_Lowest Bit value="3"/>

Table 2: GPR Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
2	RFU_C	R	0x0	nack pre divide acknowledge status (active high) <raw_Lowest Bit value="2"/>
1	RFU_B	R	0x0	mack feedback divide acknowledge status (active high) <raw_Lowest Bit value="1"/>
0	RFU_A	R	0x0	pack post divide acknowledge status (active high) <raw_Lowest Bit value="0"/>
Offset 0x58	***GP_RESETS***			
31:8	RSD_31To8	R	0x000000	non-existent bits. Reads zero <raw_Lowest Bit value="8"/>
7	GP_DCU_RESET_N	R/W	0x0	Reset for DCU. Active low. <raw_Lowest Bit value="7"/>
6	GP_VID_RESET_VD1_N	R/W	0x0	Viddec Core Reset. Active low. <raw_Lowest Bit value="6"/>
5	GP_SND_CLK_POR_N	R/W	0x0	Sound Core master reset. Only release when clocks stable. Active low. <raw_Lowest Bit value="5"/>
4	GP_I2D_RESET_N	R/W	0x0	Active Low I2D reset <raw_Lowest Bit value="4"/>
3	GP_SND_RESET27_N	R/W	0x0	Sound Core reset for 27MHz clock domain. Active low. <raw_Lowest Bit value="3"/>
2	GP_SND_RESET135_N	R/W	0x0	Sound Core reset for 13.5MHz clock domain. Active low. <raw_Lowest Bit value="2"/>
1	GP_SND_RESET675_N	R/W	0x0	Sound Core reset for 6.75MHz clock domain. Active low. <raw_Lowest Bit value="1"/>
0	GP_ITU656_RESET_N	R/W	0x0	ITU656 Formatter Active low. <raw_Lowest Bit value="0"/>
Offset 0x5C	***RFU_28***			
31:24	RSD_31To24	R	0x00	non-existent bits. Reads zero <raw_Lowest Bit value="24"/>
23:16	RFU_C	R/W	0xFF	Reserved for Future Use <raw_Lowest Bit value="16"/>
15:5	RFU_B	R/W	0x7FF	Reserved for Future Use <raw_Lowest Bit value="5"/>
4:0	RFU_A	R/W	0x1F	Reserved for Future Use <raw_Lowest Bit value="0"/>
Offset 0x60	***GP_TIMEBASE_1***			
31:27	RSD_31To27	R	0x00	non-existent bits. Reads zero <raw_Lowest Bit value="27"/> <raw_Reset By value="pi_reset_hrd_n"/>
26:19	GP_TIMEBASE_1_PH1SHIFT	R/W	0x00	shift vector for phase at phase-detector <raw_Lowest Bit value="19"/>
18:15	GP_TIMEBASE_1_KP	R/W	0xC	shift value for proportional gain factor kp <raw_Lowest Bit value="15"/>
14:11	GP_TIMEBASE_1_KI	R/W	0x4	shift value for integral gain factor ki <raw_Lowest Bit value="11"/>
10:7	GP_TIMEBASE_1_KIF	R/W	0x1	gain factor for frequency detector <raw_Lowest Bit value="7"/>
6:5	GP_TIMEBASE_1_LINE_SEL	R/W	0x1	number of lines ,Äô,Äô00,Äô = 525; ,Äô01,Äô = 625; ,Äô10,Äô = 1125; ,Äô11,Äô = reserved <raw_Lowest Bit value="5"/>
4:3	GP_TIMEBASE_1_FH_SEL	R/W	0x0	horizontal frequency select: ,Äô00,Äô = 15.525 kHz; ,Äô01,Äô = 31.25 Khz; ,Äô10,Äô = 33.75 kHz; ,Äô11,Äô = reserved <raw_Lowest Bit value="3"/>

Table 2: GPR Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
2	GP_TIMEBASE_1_INTERLACED	R/W	0x1	0 = progressive; 1 = interlaced <raw_Lowest Bit value="2"/>
1	GP_TIMEBASE_1_BYPASS	R/W	0x1	bypass PLL <raw_Lowest Bit value="1"/>
0	GP_TIMEBASE_1_FNOM	R/W	0x0	switch dto_flyback to nominal frequency <raw_Lowest Bit value="0"/>
Offset 0x64	***GP_TIMEBASE_2***			
31:28	RSD_31To28	R	0x0	non-existent bits. Reads zero <raw_Lowest Bit value="28"/>
27	GP_TIMEBASE_2_SI	R	0x0	sync_lock: 1 = locked; 0 = unlocked <raw_Lowest Bit value="27"/>
26:19	GP_TIMEBASE_2_VCR_DET	R	0x00	maximum phase error within interval of 10 fields <raw_Lowest Bit value="19"/>
18:0	GP_TIMEBASE_2_PHI1_SAW	R	0x00000	phi1_saw <raw_Lowest Bit value="0"/>
Offset 0x80	***GP_DTM_M_STAB***			
31:2	RSD_31To2	R	0x00000000	non-existent bits. Reads zero <raw_Lowest Bit value="2"/>
1:0	Gp_dtm_m_stab_b	R/W	0x0	dtl to module meta stability control <raw_Lowest Bit value="0"/> <raw_Reset By value="pi_reset_hrd_n"/>
Offset 0x84	***GP_MTD_M_STAB***			
31:2	RSD_31To2	R	0x00000000	non-existent bits. Reads zero <raw_Lowest Bit value="2"/>
1:0	Gp_mtd_m_stab_b	R/W	0x0	module to dtl meta stability control <raw_Lowest Bit value="0"/> <raw_Reset By value="pi_reset_hrd_n"/>
Offset 0xF00	***GP_VCBCONTROL***			
31:5	RSD_31To5	R	0x0000000	non-existent bits. Reads zero *REF[1] <raw_Lowest Bit value="5"/>
4:2	GP_DB_VERSION	R/W	0x0	Debug value of Version Wires <raw_Lowest Bit value="2"/>
1	GP_OR_VERSION	R/W	0x0	'1': Overrule Version Wires with DB_VERSION, '0': Normal operation <raw_Lowest Bit value="1"/>
0	GP_OR_FUNCTIONS	R/W	0x0	'1': Overrule Function Enables with DB_FUNCTIONS, '0': Normal operation <raw_Lowest Bit value="0"/>
Offset 0xF04	***GP_VCBFUNCTIONS_L***			
31:0	GP_DB_FUNCTIONS_31_0	R/W	0x00000000	Debug value of Function Enables (lower 32 bits) *REF[1] <raw_Lowest Bit value="0"/>
Offset 0xF08	***GP_VCBFUNCTIONS_H***			
31:9	RSD_31To9	R	0x000000	non-existent bits. Reads zero *REF[1] <raw_Lowest Bit value="9"/>
8:0	GP_DB_FUNCTIONS_40_32	R/W	0x000	Debug value of Function Enables (upper 9 bits) <raw_Lowest Bit value="0"/>
Offset 0xF0C	***GP_VCBVERSION_OUT***			
31:3	RSD_31To3	R	0x00000000	non-existent bits. Reads zero *REF[1] <raw_Lowest Bit value="3"/>
2:0	GP_VERSION_OUT	R	0x0	VCB Version Wire Outputs <raw_Lowest Bit value="0"/>

Table 2: GPR Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
Offset 0xF10	***GP_VCBFUNC_OUT_L***			
31:0	GP_FUNCTIONS_OUT_31_0	R	0x00003FFF	VCB Function Enable Outputs (lower 32 bits) *REF[1] <raw_Lowest Bit value="0"/>
Offset 0xF14	***GP_VCBFUNC_OUT_H***			
31:9	RSD_31To9	R	0x000000	non-existent bits. Reads zero *REF[1] <raw_Lowest Bit value="9"/>
8:0	GP_FUNCTIONS_OUT_40_32	R	0x000	VCB Function Enable Outputs (upper 9 bits) <raw_Lowest Bit value="0"/>
Offset 0xFCC	***GP_DEBUGCFG***			
31:30	RSD_31To30	R	0x0	non-existent bits. Reads zero <raw_Lowest Bit value="30"/>
29	GP_DBGSEL	R/W	0x0	'1':debug, '0':function outputs *REF[2] <raw_Lowest Bit value="29"/>
28:24	GP_TESTRAIL_CLKSEL	R/W	0x00	Testrail_clk select *REF[2] <raw_Lowest Bit value="24"/>
23:0	GP_IOSEL	R/W	0x000000	Debug configuration '1':I/O is input '0':I/O is output *REF[2] <raw_Lowest Bit value="0"/>
Offset 0xFE0	***GP_IRQ_STAT***			
31:7	RSD_31To7	R	0x0000000	non-existent bits. Reads zero <raw_Lowest Bit value="7"/>
6	GP_ITU656_INT	R	0x0	interrupt status for FORMATTER <raw_Lowest Bit value="6"/>
5	GP_VIDDEC_INT	R	0x0	interrupt status for VIDDEC <raw_Lowest Bit value="5"/>
4	GP_I2D_INT	R	0x0	interrupt status for I2D <raw_Lowest Bit value="4"/>
3	GP_DCU_INT	R	0x0	interrupt status for DCU <raw_Lowest Bit value="3"/>
2	GP_BCU_INT	R	0x0	interrupt status for BCU <raw_Lowest Bit value="2"/>
1	GP_AUDIO_INT	R	0x0	interrupt status for AUDIO DSP <raw_Lowest Bit value="1"/>
0	GP_DEMDEC_INT	R	0x0	interrupt status for DEMDEC DSP <raw_Lowest Bit value="0"/>
Offset 0xFE4	***GP_IRQ_ENAB***			
31:7	RSD_31To7	R	0x0000000	non-existent bits. Reads zero <raw_Lowest Bit value="7"/>
6:0	Gp_irq_enab_b	R/W	0x00	enable one or more interrupt requests '0' off, '1' on <raw_Lowest Bit value="0"/>
Offset 0xFE8	***GP_IRQ_CLR***			
31:7	RSD_31To7	W	0x0000000	non-existent bits. Read returns error <raw_Lowest Bit value="7"/>
6:0	Gp_irq_clr_b	W	0x00	clear one or more interrupt requests '0' off, '1' on <raw_Lowest Bit value="0"/>
Offset 0xFEC	***GP_IRQ_SET***			
31:7	RSD_31To7	W	0x0000000	non-existent bits. Read returns error <raw_Lowest Bit value="7"/>
6:0	Gp_irq_set_t	W	0x00	set one or more interrupt requests '0' off, '1' on <raw_Lowest Bit value="0"/>

Table 2: GPR Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
Offset 0xFFC	***GP_MODULE_ID***			
31:16	ID	R	0xA012	DVP module identification number <raw_Lowest Bit value="16"/>
15:12	MAJOR_REV	R	0x3	Any revision number that may break software <raw_Lowest Bit value="12"/>
11:8	MINOR_REV	R	0x0	Any revision that keep software <raw_Lowest Bit value="8"/ >
7:0	APERTURE	R	0x00	Aperture size 4kBytes <raw_Lowest Bit value="0"/>

Chapter 6: I²D Registers

PNX2000

Rev. 01 — 15 December 2003

1. I²D Register Descriptions

Table 1: I²D Register Summary

Offset	Name	Description
0x0	RX_CTRL	Settings for analogue receiver
0x4	RX_STATUS	Status of analogue receiver
0x10	I2D_DTM_M_STAB	Number of flip flops for synchronization of the read and write access to I2D config register.
0x14	I2D_MTD_M_STAB	I2D number of flip flops for synchronization of the read and write access from I2D config register to the DTL target Controller.
0x18	REC_DEMUX_MODE	Demux settings
0x1C	REC_SYNC_LOST	Sync lost timer before generating an interrupt
0x20	PRBS_STAT	Pseudo Random Bit Sequence checksum status
0x24	PRBS_CTRL	Pseudo Random Bit Sequence checksum settings
0xFE0	I2D_INT_STATUS	Status of (possible) DVP interrupt requests
0xFE4	I2D_INT_ENABLE	Enable the DVP interrupt for request to the system irq controller
0xFE8	I2D_INT_CLEAR	Clear a DVP interrupts
0xFEC	I2D_INT_SET	Set a DVP interrupt
0xFFC	I2D_MOD_ID	Block information

Table 2: I²D Registers

Bit	Symbol	Access	Reset Value	Description
Offset 0x0	*RX_CTRL*			
31:1	RSD_31To1	R/W	0x00000000	reserved
0	RX_APPL_PD	R/W	0x1	Power down for analog receiver in application mode. '0' : The analog receiver is active (normal mode) '1' : The analog receiver is in power down mode (For ADOC sleep/coma modes)
Offset 0x4	*RX_STATUS*			
31:28	RSD_31To28	R/W	0x0	reserved
27:16	RX_DC_MON	R	0xXXX	Internal DC testmode monitor point
15:2	RSD_15To2	R/W	0x0000	reserved
1	PD_STAT_STIMGEN	R	0x1	Power down monitor of internal testmode '1' : internal tester is powered down '0' : internal tester is active

Table 2: I²D Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
0	PD_STAT_RX	R	0x1	Power down monitor of analog receivers '1' : analogue receiver is powered down '0' : analog receiver is active
Offset 0x10	***I2D_DTM_M_STAB***			
31:2	RSD_31To2	R/W	0x00000000	reserved
1:0	DTL_I2D_CTRL	R/W	0x0	Number of flip flops used for synchronization during validation. Located between DTL target Ctrl to I2D '00' Have two metastability registers. '01' Have one register, bypass the other one. '1x' Bypass both metastability registers.
Offset 0x14	***I2D_MTD_M_STAB***			
31:2	RSD_31To2	R/W	0x00000000	reserved
1:0	I2D_DTL_CTRL	R/W	0x0	Number of flip flops used for synchronization during validation. Located between I2D to DTL ctrl '00' Have two metastability registers. '01' Have one register, bypass the other one. '1x' Bypass both metastability registers.
Offset 0x18	***REC_DEMUX_MODE***			
31:18	RSD_31To18	R/W	0x0000	reserved
17	I2D_SOFT_RESET	W	0x0	Softreset of the clock domain separator
16	I2D_RX_DATA_VALID_MASK	R/W	0x1	Mask the overall data valid flag inside the I2D (dv from the Clock Domain Separator). Advised not to use. '1' Enable '0' Hide
15:12	RSD_15To12	R/W	0x0	reserved
11:3	I2D_DEMUX_VALID_MASK	R/W	0x1FF	Mask data valid of the several I2D outputs. Each bit: '0' to hide the valid signal. [11] SIF [10] Right 2 [9] Left 2 [8] Right 1 [7] Left 1 [6] CVBS sec [5] U [4] Y [3] CVBS
2:0	DEMUX_MODE	R/W	0x1	Select the I2D content format to output mode '000' mode 0a '001' mode 0b '010' mode 1 '100' mode 2 '110' mode 3
Offset 0x1C	***REC_SYNC_LOST***			
31:16	DV_MISS_MAX	R/W	0x03E8	Number of consecutive valid pulses missing before generating an dv error interrupt '0' disables detection and/or resets the counter To ensure proper counting during lowering this value, first write a value of 0 into the max value, before lowering this marker. Otherwise the hold counter marker might be shifted over the counter what will result in a 16 bits overcount (afterwards it will continue at 0).
15:0	OOW_MAX	R/W	0x03E8	Number of consecutive valid pulses out of the catching window before generating an 'out of sync' (sync lost) interrupt '0' disables detection and/or resets the counter To ensure proper counting during lowering this value, first write a value of 0 into the max value, before lowering this marker. Otherwise the hold counter marker might be shifted over the counter what will result in a 16 bits overcount (afterwards it will continue at 0).
Offset 0x20	***PRBS_STAT***			
31:7	RSD_31To7	R	0x0000000	reserved
6	DV_UNDET	R	0x1	Global data valid undetected '1' DV undeteced yet '0' DV has been detected

Table 2: I²D Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
5	DV3_UNDET	R	0x1	Data valid of datalink 3 undetected '1' DV undeteced yet '0' DV has been detected
4	DV2_UNDET	R	0x1	Data valid of datalink 2 undetected '1' DV undeteced yet '0' DV has been detected
3	DV1_UNDET	R	0x1	Data valid of datalink 1 undetected '1' DV undeteced yet '0' DV has been detected
2	DLINK3_ERROR	R	0x0	Error on datalink 3
1	DLINK2_ERROR	R	0x0	Error on datalink 2
0	DLINK1_ERROR	R	0x0	Error on datalink 1
Offset 0x24	***PRBS_CTRL***			
31:8	RSD_31To8	R/W	0x000000	reserved
7	PRBS_ENABLE	R/W	0x0	Enable check on Pseudo Random Bit Sequence
6	DV_UNDET_SET	W	0x0	Set data valid detection status to undetected for global dv
5	DV3_UNDET_SET	W	0x0	Set data valid detection status to undetected for datalink 3
4	DV2_UNDET_SET	W	0x0	Set data valid detection status to undetected for datalink 2
3	DV1_UNDET_SET	W	0x0	Set data valid detection status to undetected for datalink 1
2	DL3_ERR_RST	W	0x0	Clear error status bit of datalink 3
1	DL2_ERR_RST	W	0x0	Clear error status bit of datalink 2
0	DL1_ERR_RST	W	0x0	Clear error status bit of datalink 1
Offset 0xFE0	***I2D_INT_STATUS***			
31:6	RSD_31To6	R/W	0x0000000	reserved
5	DV3_MISS_STAT	R	0x0	Data valids are missing for datalink 3 The max value dv_miss_max has been reached.
4	SYNC3_LOST_STAT	R	0x0	Data valid out of sync indication for datalink 3 The max value oow_max for out of window dv pulses has been reached.
3	DV2_MISS_STAT	R	0x0	Data valids are missing for datalink 2 The max value dv_miss_max has been reached.
2	SYNC2_LOST_STAT	R	0x0	Data valid out of sync indication for datalink 2 The max value oow_max for out of window dv pulses has been reached.
1	DV1_MISS_STAT	R	0x0	Data valids are missing for datalink 1 The max value dv_miss_max has been reached.
0	SYNC1_LOST_STAT	R	0x0	Data valid out of sync indication for datalink 1 The max value oow_max for out of window dv pulses has been reached.
Offset 0xFE4	***I2D_INT_ENABLE***			
31:6	RSD_31To6	R/W	0x0000000	reserved
5	DV3_MISS_ENA	R/W	0x0	Enable interrupt for out of window indication for datalink 3
4	SYNC3_LOST_ENA	R/W	0x0	Enable interrupt for lost of sync of datalink 3
3	DV2_MISS_ENA	R/W	0x0	Enable interrupt for out of window indication for datalink 2
2	SYNC2_LOST_ENA	R/W	0x0	Enable interrupt for lost of sync of datalink 2
1	DV1_MISS_ENA	R/W	0x0	Enable interrupt for out of window indication for datalink 1
0	SYNC1_LOST_ENA	R/W	0x0	Enable interrupt for lost of sync of datalink 1

Table 2: I²D Registers *…Continued*

Bit	Symbol	Access	Reset Value	Description
Offset 0xFE8	***I2D_INT_CLEAR***			
31:6	RSD_31To6	R/W	0x0000000	reserved
5	DV3_MISS_CLR	W	0x0	Clear indication for data valid out of window for datalink 3
4	SYNC3_LOST_CLR	W	0x0	Clear indication for lost of sync of datalink 3
3	DV2_MISS_CLR	W	0x0	Clear indication for data valid out of window for datalink 2
2	SYNC2_LOST_CLR	W	0x0	Clear indication for lost of sync of datalink 2
1	DV1_MISS_CLR	W	0x0	Clear indication for data valid out of window for datalink 1
0	SYNC1_LOST_CLR	W	0x0	Clear indication for lost of sync of datalink 1
Offset 0xFEC	***I2D_INT_SET***			
31:6	RSD_31To6	R/W	0x0000000	reserved
5	DV3_MISS_SET	W	0x0	Set indication for data valid out of window for datalink 3
4	SYNC3_LOST_SET	W	0x0	Set indication for lost of sync of datalink 3
3	DV2_MISS_SET	W	0x0	Set indication for data valid out of window for datalink 2
2	SYNC2_LOST_SET	W	0x0	Set indication for lost of sync of datalink 2
1	DV1_MISS_SET	W	0x0	Set indication for data valid out of window for datalink 1
0	SYNC1_LOST_SET	W	0x0	Set indication for lost of sync of datalink 1
Offset 0xFFC	***I2D_MOD_ID***			
31:16	I2D_MODULE_ID	R	0x0141	Module identifier
15:12	I2D_MAJOR_REV	R	0x0	Major Revision. Any revision that may break SW compatibility.
11:8	I2D_MINOR_REV	R	0x0	Minor Revision. Any revision that stillkeep SW compatibility.
7:0	I2D_APERTURE	R	0x00	Aperture Size.

Chapter 7: ITU656 Registers

PNX2000

Rev. 01 — 15 December 2003

1. ITU656 Register Descriptions

Table 1: ITU656 Register Summary

Offset	Name	Description
0x0	CONFIG	Provides IP configuration
0x4	DATA_IDToVBI	ANC VBI Data ID
0x8	DATA_IDToHBI	ANC HBI Data ID
0xC	CAPTURE	Capture parameters
0x10	FIFO	FIFO Register
0x14	VF_CONTROL	VF CONTROL Register
0x18	VF_SYNC	VF SYNC Register
0x1C	FIELD_1	FIELD 1 register
0x20	FIELD_2	FIELD 2 register
0x24	VBI_1	VBI 1 register
0x28	VBI_2	VBI 2 register
0x2C	VBI_3	VBI 3 register
0x30	VBI_4	VBI 4 register
0x34	PROG_HBI	Prog HBI register
0x38	YUV_Offset	Prog HBI register
0xFC4	DTM_SYNC	DTL to module Metastability
0xFC8	MTD_SYNC	Module to DTL Metastability
0xFCC	DEBUG	Debug control
0xFE0	INT_STATUS	Interrupt Status
0xFE4	INT_ENABLE	Interrupt Enable
0xFE8	INT_CLEAR	Interrupt Clear
0xFEC	INT_SET	Interrupt Set
0xFFC	MODULE_ID	ITU656 formatter ID

Table 2: ITU656 Registers

Bit	Symbol	Access	Reset Value	Description
Offset 0x0	*CONFIG*			
31:16	RSD_31To16	R	0x0000	Unused <raw_Reset By value="reset_viddec_n"/>
15	DVO_ENABLE	R/W	0x0	1=DVO outputs enabled <raw_Reset By value="reset_viddec_n"/>
14	INPUT_TEST_MODE	R/W	0x0	1=Output mono bar test pattern <raw_Reset By value="reset_viddec_n"/>
13	OUTPUT_TEST_MODE	R/W	0x0	1=Output colour bar test pattern <raw_Reset By value="reset_viddec_n"/>
12	PROGESSIVE_MODE	R/W	0x0	1=Progressive mode, timing flags always 1st field <raw_Reset By value="reset_viddec_n"/>
11	CLOCK_STUTTER	R/W	0x0	1=ITU clock stuttered <raw_Reset By value="reset_viddec_n"/>
10	CLOCK_INVERT	R/W	0x0	1=ITU data clocked from Formatter on rising edge <raw_Reset By value="reset_viddec_n"/>
9	DC_JUSTIFIED	R/W	0x0	1=VBI ANC Data Count justified to an integer number of 4 blocks, for usage in 8-bit ITU <raw_Reset By value="reset_viddec_n"/>
8	DITHER	R/W	0x0	1=LSB of 9-bit video will be dithered into 8-bit ITU <raw_Reset By value="reset_viddec_n"/>
7	UV_COMPL	R/W	0x0	1=MSB of 9-bit UV video willl be inverted <raw_Reset By value="reset_viddec_n"/>
6	CVBS_COMPL	R/W	0x0	1=MSB of 9-bit CVBS will be inverted <raw_Reset By value="reset_viddec_n"/>
5	VBI_ONLY	R/W	0x0	1=Even during active video (non-vertical blanking) text is transmitted from the DCU and inserted into ITU data stream. <raw_Reset By value="reset_viddec_n"/>
4:3	VBI_CONTROL	R/W	0x0	Modes for Avoidance of '00' and 'FF' in data stream during VBI transmission are: '00'=Pure Text - VBI bytes are shifted left (left aligned). The risk to get an unwanted sequence with 'FF', '00', EAV/SAV is high for 8-bit recognition, but zero for 10-bit recognition, as the two LSBs are modified to prevent that. '01'=One bit wrong - (in case of 8-bit ITU) VBI bytes will be modified in the LSB bit to prevent from getting '00' or 'FF' in the data. '10'=No Test Shift - VBI bytes will not be shifted left and the two MSBs are modified to prevent from getting '00' or 'FF' (for 10-bit use). '11'=Nibble - VBI data bytes will be transmitted via two nibbles, low nibble first filled with '1010'. <raw_Reset By value="reset_viddec_n"/>
2	COLUMBUS	R/W	0x0	1=656 output data stream contains CVBS/Chrominance samples. <raw_Reset By value="reset_viddec_n"/>
1:0	MODE	R/W	0x0	See Table 1 (FRS V1.0) Supported Video Standards <raw_Reset By value="reset_viddec_n"/>
Offset 0x4	*DATA_IDToVBI*			
31:30	RSD_31To30	R	0x0	Unused <raw_Reset By value="reset_viddec_n"/>
29:20	SDID_VBI	R/W	0x000	ANC VBI SDID byte <raw_Reset By value="reset_viddec_n"/>

Table 2: ITU656 Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
19:10	DID2_VBI	R/W	0x000	ANC VBI DID byte for field 2 (even field) <raw_Reset By value="reset_viddec_n"/>
9:0	DID1_VBI	R/W	0x000	ANC VBI DID byte for field 1 (odd field) <raw_Reset By value="reset_viddec_n"/>
Offset 0x8	***DATA_IDToHBI***			
31:30	RSD_31To30	R	0x0	Unused <raw_Reset By value="reset_viddec_n"/>
29:20	SDID_HBI	R/W	0x000	ANC HBI SDID byte <raw_Reset By value="reset_viddec_n"/>
19:10	DID2_HBI	R/W	0x000	ANC HBI DID byte for field 2 (even field) <raw_Reset By value="reset_viddec_n"/>
9:0	DID1_HBI	R/W	0x000	ANC HBI DID byte for field 1 (odd field) <raw_Reset By value="reset_viddec_n"/>
Offset 0xC	***CAPTURE***			
31:30	RSD_31To30	R	0x0	Unused <raw_Reset By value="reset_viddec_n"/>
29:24	YUV_LATENCY	R/W	0x00	YUV latency from 1st byte to start of fram <raw_Reset By value="reset_viddec_n"/>
23:21	RSD_23To21	R	0x0	Unused <raw_Reset By value="reset_viddec_n"/>
20	SYNC_TO_HSYNC	R/W	0x0	1 = sync timing to HSYNC, 0 = sync to HSY_OUT <raw_Reset By value="reset_viddec_n"/>
18:8	CVBS_LATENCY	R/W	0x03E	cvbs latency <raw_Reset By value="reset_viddec_n"/>
7	RSD_Bit7	R	0x0	Unused <raw_Reset By value="reset_viddec_n"/>
6:0	CVBS_FIFO_OFFSET	R/W	0x74	cvbs fifo offset <raw_Reset By value="reset_viddec_n"/>
Offset 0x10	***FIFO***			
31:25	RSD_31To25	R	0x00	Unused <raw_Reset By value="reset_viddec_n"/>
24	FIFO_CONTROL	R/W	0x0	operate FIFO buffering <raw_Reset By value="reset_viddec_n"/>
23	RSD_Bit23	R	0x0	Unused <raw_Reset By value="reset_viddec_n"/>
22:12	FIFO_WIN_STOP	R/W	0x000	FIFO window stop value <raw_Reset By value="reset_viddec_n"/>
11	RSD_Bit11	R	0x0	Unused <raw_Reset By value="reset_viddec_n"/>
10:0	FIFO_WIN_START	R/W	0x000	FIFO window start value <raw_Reset By value="reset_viddec_n"/>
Offset 0x14	***VF_CONTROL***			
31:14	RSD_31To14	R	0x00000	Unused <raw_Reset By value="reset_viddec_n"/>
13	EAV_UPDATE	R/W	0x0	1 = Update VBI and field indicators with EAV <raw_Reset By value="reset_viddec_n"/>
12	VBI_FIELD_CONTROL	R/W	0x0	1 = Use VBI and field indicators generated within the ITU656 formatter <raw_Reset By value="reset_viddec_n"/>
11	RSD_Bit11	R	0x0	Unused <raw_Reset By value="reset_viddec_n"/>
10:0	LINE_NUMBER	R/W	0x271	Quantity of lines per frame <raw_Reset By value="reset_viddec_n"/>
Offset 0x18	***VF_SYNC***			
31:23	RSD_31To23	R	0x000	Unused <raw_Reset By value="reset_viddec_n"/>

Table 2: ITU656 Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
22:12	SYNC_VALUE_F1	R/W	0x13C	sync value for field one (F1) <raw_Reset By value="reset_viddec_n"/>
11	RSD_Bit11	R	0x0	Unused <raw_Reset By value="reset_viddec_n"/>
10:0	SYNC_VALUE_F0	R/W	0x003	sync value for field one (F0) <raw_Reset By value="reset_viddec_n"/>
Offset 0x1C	***FIELD_1***			
31:23	RSD_31To23	R	0x000	Unused <raw_Reset By value="reset_viddec_n"/>
22:12	FIELD_STOP_1	R/W	0x271	field stop value <raw_Reset By value="reset_viddec_n"/>
11	RSD_Bit11	R	0x0	Unused <raw_Reset By value="reset_viddec_n"/>
10:0	FIELD_START_1	R/W	0x138	field start value (+1) <raw_Reset By value="reset_viddec_n"/>
Offset 0x20	***FIELD_2***			
31:23	RSD_31To23	R	0x000	Unused <raw_Reset By value="reset_viddec_n"/>
22:12	FIELD_STOP_2	R/W	0x003	field stop value <raw_Reset By value="reset_viddec_n"/>
11	RSD_Bit11	R	0x0	Unused <raw_Reset By value="reset_viddec_n"/>
10:0	FIELD_START_2	R/W	0x13C	field start value (+1) <raw_Reset By value="reset_viddec_n"/>
Offset 0x24	***VBI_1***			
31:23	RSD_31To23	R	0x000	Unused <raw_Reset By value="reset_viddec_n"/>
22:12	VBI_STOP_1	R/W	0x14F	VBI stop value <raw_Reset By value="reset_viddec_n"/>
11	RSD_Bit11	R	0x0	Unused <raw_Reset By value="reset_viddec_n"/>
10:0	VBI_START_1	R/W	0x136	VBI start value (+1) <raw_Reset By value="reset_viddec_n"/>
Offset 0x28	***VBI_2***			
31:23	RSD_31To23	R	0x000	Unused <raw_Reset By value="reset_viddec_n"/>
22:12	VBI_STOP_2	R/W	0x016	VBI stop value <raw_Reset By value="reset_viddec_n"/>
11	RSD_Bit11	R	0x0	Unused <raw_Reset By value="reset_viddec_n"/>
10:0	VBI_START_2	R/W	0x26F	VBI start value (+1) <raw_Reset By value="reset_viddec_n"/>
Offset 0x2C	***VBI_3***			
31:23	RSD_31To23	R	0x001	Unused <raw_Reset By value="reset_viddec_n"/>
22:12	VBI_STOP_3	R/W	0x7FF	VBI stop value <raw_Reset By value="reset_viddec_n"/>
11	RSD_Bit11	R	0x0	Unused <raw_Reset By value="reset_viddec_n"/>
10:0	VBI_START_3	R/W	0x003	VBI start value (+1) <raw_Reset By value="reset_viddec_n"/>
Offset 0x30	***VBI_4***			
31:23	RSD_31To23	R	0x001	Unused <raw_Reset By value="reset_viddec_n"/>
22:12	VBI_STOP_4	R/W	0x7FF	VBI stop value <raw_Reset By value="reset_viddec_n"/>
11	RSD_Bit11	R	0x0	Unused <raw_Reset By value="reset_viddec_n"/>
10:0	VBI_START_4	R/W	0x13C	VBI start value (+1) <raw_Reset By value="reset_viddec_n"/>

Table 2: ITU656 Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
Offset 0x34	***PROG_HBI***			
31:22	HBI_DC	R/W	0x000	Horizontal blanking interval data count value <raw_Reset By value="reset_viddec_n"/>
21:11	CB_OFF_SLOT	R/W	0x000	colour burst off slot <raw_Reset By value="reset_viddec_n"/>
10:0	SAV_SLOT	R/W	0x7B8	first sav slot <raw_Reset By value="reset_viddec_n"/>
Offset 0x38	***YUV_Offset***			
31:22	RSD_31To22	R	0x000	Unused <raw_Reset By value="reset_viddec_n"/>
21:16	V_OFFSET	R/W	0x00	V offset value <raw_Reset By value="reset_viddec_n"/>
15:14	RSD_15To14	R	0x0	Unused <raw_Reset By value="reset_viddec_n"/>
13:8	U_OFFSET	R/W	0x00	U offset value <raw_Reset By value="reset_viddec_n"/>
7:6	RSD_7To6	R	0x0	Unused <raw_Reset By value="reset_viddec_n"/>
5:0	Y_OFFSET	R/W	0x00	Y offset value <raw_Reset By value="reset_viddec_n"/>
Offset 0xFC4	***DTM_SYNC***			
31:2	RSD_31To2	R	0x00000000	Unused <raw_Reset By value="reset_viddec_n"/>
1:0	DTM_SYNC_D	R/W	0x0	Metastability control <raw_Reset By value="reset_viddec_n"/>
Offset 0xFC8	***MTD_SYNC***			
31:2	RSD_31To2	R	0x00000000	Unused <raw_Reset By value="reset_viddec_n"/>
1:0	MTD_SYNC_M	R/W	0x0	Metastability control <raw_Reset By value="reset_viddec_n"/>
Offset 0xFCC	***DEBUG***			
31:3	RSD_31To3	R	0x00000000	Unused <raw_Reset By value="reset_viddec_n"/>
2:1	DEBUG_SEL	R/W	0x0	debug rail selection <raw_Reset By value="reset_viddec_n"/>
0	DEBUG_OUTPUT_SELECT	R/W	0x0	debug output select <raw_Reset By value="reset_viddec_n"/>
Offset 0xFE0	***INT_STATUS***			
31:1	RSD_31To1	R	0x00000000	Unused <raw_Reset By value="reset_viddec_n"/>
0	DCU_BUF_INT_STATUS	R	0x0	Interrupt status of DCU buffers <raw_Reset By value="reset_viddec_n"/>
Offset 0xFE4	***INT_ENABLE***			
31:1	RSD_31To1	R	0x00000000	Unused <raw_Reset By value="reset_viddec_n"/>
0	DCU_BUF_INT_ENABLE	R/W	0x0	Enable interrupt DCU buffers <raw_Reset By value="reset_viddec_n"/>
Offset 0xFE8	***INT_CLEAR***			
31:1	RSD_31To1	W	0x00000000	Unused <raw_Reset By value="reset_viddec_n"/>
0	DCU_BUF_INT_CLEAR	W	0x0	Clear interrupt DCU buffers <raw_Reset By value="reset_viddec_n"/>
Offset 0xFEC	***INT_SET***			
31:1	RSD_31To1	W	0x00000000	Unused <raw_Reset By value="reset_viddec_n"/>

Table 2: ITU656 Registers *…Continued*

Bit	Symbol	Access	Reset Value	Description
0	DCU_BUF_INT_SET	W	0x0	Set interrupt DCU buffers <raw_Reset By value="reset_viddec_n"/>
Offset 0xFFC	***MODULE_ID***			
31:16	ID	R	0xA05F	Module ID. This field identifies the block as type ITU656 formatter. <raw_Reset By value="reset_viddec_n"/>
15:12	MAJ_REV	R	0x0	Major revision ID. Breaks S/W compatibility. This field is incremented by 1 when a change introduced into the block results in software incompatibility with the previous version of the block. First version default = 0. <raw_Reset By value="reset_viddec_n"/>
11:8	MIN_REV	R	0x0	Minor revision ID. Keeps S/W compatibility.This field is incremented by 1 when a change introduced into the block maintains software compatibility with the previous version of the block. First version default = 0. <raw_Reset By value="reset_viddec_n"/>
7:0	APERTURE	R	0x00	Aperture size. Identifies the MMIO aperture size in units of 4KB. The ITU656 formatter has an aperture size of 4KB. Aperture = 0; 4KB. <raw_Reset By value="reset_viddec_n"/>

Chapter 8: PI_1003_BCU Registers

PNX2000

Rev. 01 — 15 December 2003

1. PI_1003_BCU Register Descriptions

Table 1: PI_1003_BCU Register Summary

Offset	Name	Description
0x0	INT_STATUS	BCU interrupt status
0x4	INT_SET	BCU interrupt set
0x8	INT_CLEAR	BCU interrupt clear
0xC	FAULT_STATUS	Bus fault status
0x10	FAULT_ADDRESS	Bus fault address
0x14	INT_ENABLE	BCU interrupt enable
0x18	TOUT	Time-out control
0x1C	SNOOP	Memory coherency control

Table 2: PI_1003_BCU Registers

Bit	Symbol	Access	Reset Value	Description
Offset 0x0	*INT_STATUS*			
31:2	RSD_31To2	R	0x00000000	Reserved
1	BCU_TO_STATUS	R	0x0	Time-out status: '0' = no time-out error has occurred. '1' = time-out error has occurred
0	BCU_BE_STATUS	R	0x0	Bus error status: '0' = no bus error has occurred. Fault logging enabled if BCU_TO=0 and BCU_BE=0; '1' = bus error has occurred, Fault logging stopped.
Offset 0x4	*INT_SET*			
31:2	RSD_31To2	R	0xXXXXXXXX	Reserved
1	BCU_TO_SET	W	0xX	Write '1' to set Time-Out interrupt; '0' has no effect
0	BCU_BE_SET	W	0xX	Write '1' to set Bus-Error interrupt; '0' has no effect
Offset 0x8	*INT_CLEAR*			
31:2	RSD_31To2	R	0xXXXXXXXX	Reserved
1	BCU_TO_CLEAR	W	0xX	Write '1' to clear Time-Out interrupt; '0' has no effect
0	BCU_BE_CLEAR	W	0xX	Write '1' to clear Bus-Error interrupt; '0' has no effect
Offset 0xC	*FAULT_STATUS*			
31:15	RSD_31To15	R	0xXXXXX	Reserved

Table 2: PI_1003_BCU Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
14:7	BCU_MASTER	R	0xXX	Bus master of failed bus operation: 1 = Bus master 0; 2 = Bus master 1; 3 = Bus master 2; 4 = Bus master 3; &H10 = Bus master 4; &H20 = Bus master 5; &H40 = Bus master 6; &H80 = Bus master 7
6	BCU_LOCK	R	0xX	Lock status of failed bus operation: '0' = LOCK was 0; '1' = LOCK was 1
5	BCU_READ	R	0xX	Data direction of failed bus operation: 0 = write operation; 1 = read operation
4:0	BCU_OPC	R	0xXX	Opcode of failed operation
Offset 0x10	***FAULT_ADDRESS***			
31:2	BCU_ADDR	R	0xXXXXXXXX	Address of failed bus operation
1:0	RSD_1To0	R	0x0	Reserved. Returns '0' on read.
Offset 0x14	***INT_ENABLE***			
31:1	RSD_31To1	R	0x00000000	Reserved
0	BCU_INT_EN	R/W	0x0	'0' = disable BCU interrupt request; '1' = enable interrupt request - an interrupt is generated when BCU_TO and/or BCU_BE flag is set
Offset 0x18	***TOUT***			
31:0	BCU_TO_THRESHOLD	R/W	0x00000000	Time-out threshold: '0' = never time-out; '1' = time-out after 1st data cycle in bus operation; ,Ä¶; 255 = time-out after 256th data cycle in bus operation
Offset 0x1C	***SNOOP***			
31:10	RSD_31To10	R	0x000000	Reserved
9:2	BCU_SNOOP_MASTERS	R/W	0x00	Snoop on masters: Bit 0 corresponds to master 0, ,Ä¶, bit 7 corresponds to master 7; '1' on each bit to enable snooping
1	BCU_SNOOP_WRITE	R/W	0x0	Snoop on write: '0' = disable snoop on write; '1' = enable snoop on write
0	BCU_SNOOP_READ	R/W	0x0	Snoop on read: '0' = disable snoop on read; '1' = enable snoop on read

Chapter 9: VIDDEC Registers

PNX2000

Rev. 01 — 15 December 2003

1. VIDDEC Register Descriptions

Table 1: VIDDEC Register Summary

Offset	Name	Description
0x0	Viddec_status10	Status register 1
0x4	Viddec_status20	Status register 2
0x8	Agc_status_hw_gain0	AGC Status Register
0x40	Mux00	Mux control (Miscellaneous)
0x80	Agc_sync_amp0	AGC Sync Amplifier control
0x84	Agc_cvbs_yyc_amp0	AGC CVBS & Yyc amplifier control
0x88	Agc_y_cyc_amp0	AGC Ycrcb&Cyc Amplifier control
0x8C	Agc_crcb_amp0	AGC CrCb Amplifier control
0x90	Agc_sync_control0	AGC control of sync control block
0x94	Agc_cvbs_yyc_control0	AGC control of cvbs&Yyc control block
0x98	Agc_y_cyc_control0	AGC control of Ycrcb&Cyc control block
0x9C	Agc_y_cyc_targets0	AGC target levels for Ycrcb&Cyc control loop
0xA0	Agc_lower_gain_limits0	AGC lower gain limits for each control block
0xA4	Agc_upper_gain_limits0	AGC upper gain limits for each control block
0xC0	Fstblnk0	Fast blank YUV delay
0x100	Hv_info_10	HV Info 1
0x104	Hv_info_20	HV Info 2
0x108	Hv_info_30	HV Info 3
0x10C	Hv_info_40	HV Info 4
0x140	Subpix_2fhpllsync00	subpix_2fhpll sync register 0
0x144	Subpix_2fhpllsync10	subpix_2fhpll sync register 1
0x148	Subpix_2fhpllsync20	subpix_2fhpll sync register 2
0x14C	Subpix_2fhpllsync30	subpix_2fhpll sync register 3
0x180	Dmsd_h_sync0	
0x184	Dmsd_v_sync0	
0x188	Dmsd_std_det0	
0x18C	Dmsd_col_dec0	
0x190	Dmsd_filters0	
0x194	Dmsd_outputs0	

Table 1: VIDDEC Register Summary *...Continued*

Offset	Name	Description
0x198	Dmsd_misc0	
0x300	Dtm_mstab0	
0x304	Mtd_mstab0	
0x308	Copy_buffer0	
0xFCC	Debugctrl0	
0xFE0	Viddec_int_cond0	Interrupt conditions to dtl controller
0xFE4	Viddec_irq_enab0	
0xFE8	Viddec_irq_clr0	
0xFEC	Viddec_irq_set0	
0xFFC	Viddec_id0	Module ID

Table 2: VIDDEC Registers

Bit	Symbol	Access	Reset Value	Description
Offset 0x0	***Viddec_status10***			
31:12	RSD_31To12	R	0x00000	Reserved
11	Dmsd_nfld	R	0xX	nominal field length video input signal
10	Dmsd_tvdet	R	0xX	stability indicator for timebase of input signal
9	Dmsd_type3	R	0xX	
8	Dmsd_colstr	R	0xX	
7:0	Dmsd_acgain	R	0xXX	Status of internal chroma gain control
Offset 0x4	***Viddec_status20***			
31:26	RSD_31To26	R	0x00	Reserved
25:23	Ver_meas_2fh	R	0xX	2fH number of lines per field found (coded)
22:21	Hor_meas_2fh	R	0xX	2fH number of pixels per line found (coded)
20	Meas_atsc_2fh	R	0xX	2fH atsc identification
19	Meas_intl_2fh	R	0xX	2fH interlacing identification
18	Fastblank_in2	R	0xX	level at fast blank input 2 during vsync
17	Fastblank_in1	R	0xX	level at fast blank input 1 during vsync
16	Fidt_2fh	R	0xX	field frequency as detected by 2fH loop; 0=50Hz
15	Dtc_tdc_lock	R	0xX	glitch filtered dll lock signal; 1=in lock
14	Dll_lock	R	0xX	dll lock indicator of analogue part
13	Dto_atsc	R	0xX	‚Äò1‚Äô:ATSC source detected; valid when in lock and in 2fH mode
12	Copro_2fh	R	0xX	‚Äò1‚Äô copy protection detected in 2fh input signal
11	Intl_2fh	R	0xX	subpix_2fhpll_int ‚Äò0‚Äô noninterlaced
10	Vl_2fh	R	0xX	‚Äò1‚Äô 2 FH vertical lock
9	Hl_2fh	R	0xX	
8	Dmsd_hnoise	R	0xX	‚Äò1‚Äô noise detected during sync bottom

Table 2: VIDDEC Registers *…Continued*

Bit	Symbol	Access	Reset Value	Description
7:6	Dmsd_ftvs	R	0xX	,Äú00,Äù BlackWhite ,Äú01,Äù NTSC ,Äú10,Äù PAL ,Äú11,Äù SECAM
5	Dmsd_copro	R	0xX	dmsd_copro ,Äò1,Äô copy protected source detected
4	Dmsd_code	R	0xX	dmsd_code ,Äò1,Äô colour detected according standard
3	Dmsd_fidt	R	0xX	detected field freq ,Äò0,Äô 50Hz
2	Dmsd_intl	R	0xX	dmsd_intl ,Äò0,Äô noninterlaced
1	Dmsd_vl	R	0xX	,Äò1,Äô 1 FH vertical lock
0	Dmsd_hl	R	0xX	,Äò1,Äô 1 FH horizontal lock
Offset 0x8	***Agc_status_hw_gain0***			
31:30	RSD_31To30	R	0x0	Reserved
29:20	Agc_y_cyc_monitor_hw gain	R	0xXXX	gain as determined by hardware loop for Ycrcb
19:10	Agc_cvbs_yc_monitor_h wgain	R	0xXXX	gain as determined by hardware loop for CVBS&Yyc
9:0	Agc_sync_monitor_hwg ain	R	0xXXX	gain as determined by hardware loop for SYNC
Offset 0x40	***Mux00***			
31:9	RSD_31To9	R	0x000000	Reserved
8	Dtc_lowth	R/W	0x1	select low threshold for FastBlank
7	Sel_ext_vsync_2	R/W	0x0	select external vsync source
6	Even_inv	R/W	0x0	swap polarity of even field data signal for DCU
5	Ffield_inv	R/W	0x0	swap polarity of first field data signal for FBX
4	Uv_valid_inv	R/W	0x0	swap u and v info
3	Chr_inp_del	R/W	0x0	Chroma Input Select for DMSD
2	Dmsd_sync_sel_y	R/W	0x0	0,Äô cvbs or yc sync ,Äò1,Äô 1fh y internal sync
1:0	RSD_1To0	R/W	0x0	Reserved
Offset 0x80	***Agc_sync_amp0***			
31:29	Agc_sync_divider	R/W	0x6	divider value (programmable gain)
28:25	RSD_28To25	R	0x0	Reserved
24:16	Agc_sync_blanking_offs et_out	R/W	0x138	black level sync amplifier output
15:8	RSD_15To8	R	0x00	Reserved
7:0	Agc_sync_blanking_offs et_in	R/W	0x80	black level sync amplifier input
Offset 0x84	***Agc_cvbs_yyc_amp0***			
31:29	Agc_cvbs_yyc_divider	R/W	0x3	divider value (programmable gain)
28:25	RSD_28To25	R	0x0	Reserved
24:16	Agc_cvbs_yyc_blanking _offset_out	R/W	0x138	black level CVBS&Yyc amplifier output
15:8	RSD_15To8	R	0x00	Reserved

Table 2: VIDDEC Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
7:0	Agc_cvbs_yyc_blanking_offset_in	R/W	0x80	black level CVBS&Yyc amplifier input
Offset 0x88	***Agc_y_cyc_amp0***			
31:29	Agc_y_cyc_divider	R/W	0x4	divider value (programmable gain)
28:25	RSD_28To25	R	0x0	Reserved
24:16	Agc_y_cyc_blanking_offset_out	R/W	0x138	black level Ycrcb & Cyc amplifier output
15:8	RSD_15To8	R	0x00	Reserved
7:0	Agc_y_cyc_blanking_offset_in	R/W	0x80	black level Ycrcb&Cyc amplifier input
Offset 0x8C	***Agc_crcb_amp0***			
31:29	Agc_crcb_divider	R/W	0x3	divider value (programmable gain)
28:25	RSD_28To25	R	0x0	Reserved
24:16	Agc_crcb_blanking_offset_out	R/W	0x0C0	black level CrCb amplifier output
15:8	RSD_15To8	R	0x00	Reserved
7:0	Agc_crcb_blanking_offset_in	R/W	0x00	black level CrCb amplifier input
Offset 0x90	***Agc_sync_control0***			
31:23	RSD_31To23	R	0x000	Reserved
22:20	Agc_sync_ctrl_tau_inlock_pi	R/W	0x6	Time Constant when ITS_Combdec has Horizontal-Lock
19	RSD_Bit19	R	0x0	Reserved
18:16	Agc_sync_ctrl_tau_catch_pi	R/W	0x1	Time Constant when ITS_Combdec has no Horizontal-Lock
15:12	RSD_15To12	R	0x0	Reserved
11	Agc_sync_ctrl_holdgain_pi	R/W	0x0	to freeze gain value
10	Agc_sync_ctrl_forcegain_pi	R/W	0x0	to force gain value by means of SW
9:0	Agc_sync_ctrl_gainvalue_pi	R/W	0x0E8	gain when agc_sync_ctrl_force_gain ='1'
Offset 0x94	***Agc_cvbs_yyc_control0***			
31:27	RSD_31To27	R	0x00	Reserved
26	Agc_cvbs_yc_ctrl_copy_prot_pi	R/W	0x0	use 80% of nominal sync amplitude as reference (macro vision)
25	Agc_cvbs_yc_ctrl_en_sync_int_pi	R/W	0x1	enable influence internal top sync det. to the AGC control loop
24	Agc_cvbs_yc_ctrl_en_pw_int_pi	R/W	0x1	enable influence internal peak white det. to the AGC control loop
23	Agc_cvbs_yc_ctrl_en_pw_ext_pi	R/W	0x1	enable influence peak white det. Of ITS_Combdec to the AGC control loop

Table 2: VIDDEC Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
22:20	Agc_cvbs_yc_ctrl_tau_inlock_pi	R/W	0x6	Time Constant when ITS_Combdec has Horizontal-Lock
19	RSD_Bit19	R	0x0	Reserved
18:16	Agc_cvbs_yc_ctrl_tau_catch_pi	R/W	0x1	Time Constant when ITS_Combdec has no Horizontal-Lock
15:12	RSD_15To12	R	0x0	Reserved
11	Agc_cvbs_yc_ctrl_holdgain_pi	R/W	0x0	to freeze gain value
10	Agc_cvbs_yc_ctrl_forcegain_pi	R/W	0x0	to force gain value by means of SW
9:0	Agc_cvbs_yc_ctrl_gainvalue_pi	R/W	0x1CD	gain when agc_sync_ctrl_force_gain ='1'
Offset 0x98	***Agc_y_cyc_control0***			
31:26	RSD_31To26	R	0x00	Reserved
25	Agc_y_cyc_ctrl_enable_sync_int_pi	R/W	0x1	enable influence internal top sync det. to the AGC control loop
24	Agc_y_cyc_ctrl_enable_pw_int_pi	R/W	0x1	enable influence internal peak white det. to the AGC control loop
23	RSD_Bit23	R	0x0	Reserved
22:20	Agc_y_cyc_ctrl_tau_inlock_pi	R/W	0x6	Time Constant when ITS_Combdec has Horizontal-Lock
19	RSD_Bit19	R	0x0	Reserved
18:16	Agc_y_cyc_ctrl_tau_catch_pi	R/W	0x1	Time Constant when ITS_Combdec has no Horizontal-Lock
15:12	RSD_15To12	R	0x0	Reserved
11	Agc_y_cyc_ctrl_holdgain_pi	R/W	0x0	to freeze gain value
10	Agc_y_cyc_ctrl_forcegain_pi	R/W	0x0	to force gain value by means of SW
9:0	Agc_y_cyc_ctrl_gainvalue_pi	R/W	0x0E8	gain when agc_sync_ctrl_force_gain ='1'
Offset 0x9C	***Agc_y_cyc_targets0***			
31:25	RSD_31To25	R	0x00	Reserved
24:16	Agc_y_cyc_ctrl_top_sync_target_pi	R/W	0x100	top sync level target for internal top sync detector
15:9	RSD_15To9	R	0x00	Reserved
8:0	Agc_y_cyc_ctrl_peak_target_pi	R/W	0x1FF	peak white level target for internal peak white detector
Offset 0xA0	***Agc_lower_gain_limits0***			
31:30	RSD_31To30	R	0x0	Reserved
29:20	Agc_y_cyc_ctrl_low_gain_lim_pi	R/W	0x11F	lower gain limit for ycrcb control loop

Table 2: VIDDEC Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
19:10	Agc_cvbs_yyc_ctrl_low_gain_lim_pi	R/W	0x142	lower gain limit for cvbs_yyc control loop
9:0	Agc_sync_ctrl_low_gain_lim_pi	R/W	0x0AB	lower gain limit for sync control loop
Offset 0xA4	***Agc_upper_gain_limits0***			
31:30	RSD_31To30	R	0x0	Reserved
29:20	Agc_y_cyc_ctrl_up_gain_lim_pi	R/W	0x332	upper gain limit for ycrcb control loop
19:10	Agc_cvbs_yyc_ctrl_up_gain_lim_pi	R/W	0x39A	upper gain limit for cvbs_yyc control loop
9:0	Agc_sync_ctrl_up_gain_lim_pi	R/W	0x2DB	upper gain limit for sync control loop
Offset 0xC0	***Fstblnk0***			
31:13	RSD_31To13	R	0x00000	Reserved
12	Fbl_polarity	R/W	0x1	0:Fast Blank high is insert; 1:Fast Blank low is insert
11:10	Fbl_switch_ctrl	R/W	0x0	00 or 11: Fast Blank pin controls switch; 01:decoder select;10:YCrCb select
9:6	Fbl_vardelay_dtl	R/W	0x0	delay figure for allignment YCrCb to Video
5	Sel_fbl_var_delay_dtl	R/W	0x0	0:autoloop figures used;1:reg figures are used
4	Sel_hsync_fbl2	R/W	0x0	0:hsync_fbl1 selected;1:hsync_fbl2 selected
3:0	Yuv2fhdelay	R/W	0x0	step size 1 active y pixel (gated_llclk1) ,Äú0000,Äù + 0 steps ,Äú1111,Äù + 15 steps
Offset 0x100	***Hv_info_10***			
31:9	RSD_31To9	R	0x000000	Reserved
8:0	Hv_info_start	R/W	0x060	Start Horizontol Timing Pulse
Offset 0x104	***Hv_info_20***			
31:9	RSD_31To9	R	0x000000	Reserved
8:0	Hv_info_length	R/W	0x048	Width Horizontol Timing Pulse
Offset 0x108	***Hv_info_30***			
31:25	RSD_31To25	R	0x00	Reserved
24	Hv_info_ignore_hl	R/W	0x1	ignore horizontal lock info for hv_info generator
23:9	RSD_23To9	R	0x0000	Reserved
8:0	Hv_info_disable	R/W	0x080	Width Horizontol Timing Pulse during lines where clamp must be disabled
Offset 0x10C	***Hv_info_40***			
31:9	RSD_31To9	R	0x000000	Reserved
8:0	Hv_info_vsync_length	R/W	0x120	Width Horizontol Timing Pulse within vertical blanking interval
Offset 0x140	***Subpix_2fhpllsync00***			
31:23	RSD_31To23	R	0x000	Reserved
22:21	Atsc_mode_2fh	R/W	0x0	Select ATSC standard (US1, US2, Australia, China)

Table 2: VIDDEC Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
20	Auto_atsc_2fh	R/W	0x0	automatically use value from HW from detection ATSC
19	Sel_atsc_2fh	R/W	0x0	select atsc H&V windows
18	Sel_intl_2fh	R/W	0x0	0 non interlaced; 1 interlaced
17	Auto_intl_2fh	R/W	0x0	1 auto detection interlaced; 0 use value from subpix_2fh_pll_sel_intl reg
16	Dtc_ignore_lock	R/W	0x0	1 Force TDC function although lock indicator states 'not in lock'
15	Ldel_2fh	R/W	0x0	To shift Vertical timing pulses wrt to Video; obsolete
14	Ycomb_2fh	R/W	0x0	To shift Vertical timing pulses wrt to Video; obsolete
13	Pal_2fh	R/W	0x0	To shift Vertical timing pulses wrt to Video; obsolete
12	Vgps_2fh	R/W	0x0	To shift position of HV_INFO Vertical interval; obsolete
11	Sel_ext_2fh	R/W	0x0	0 sync on Y; 1 external horizontal and vertical sync
10	Set_3l_2fh	R/W	0x0	0 normal sync; 1 tri-level sync for ATSC
9:6	Yuv2fbldelay	R/W	0x8	Step size 1 active y pixel (gated_llclk1) ,Äú0000,Äù + 0 steps ,Äú1111,Äù + 15 steps
5:0	RSD_5To0	R/W	0x00	Reserved
Offset 0x144	***Subpix_2fhpllsync10***			
31:24	RSD_31To24	R	0x00	Reserved
23:22	Vnoi_2fh	R/W	0x0	vertical noise reduction 00 Normal; 01 Fast; 10 Freerunning; 11 Debug only
21	Hpll_2fh	R/W	0x0	2fh PLL: 0 Normal operation (locked to the input signal); 1 freerunning
20:19	Htc_2fh	R/W	0x0	2fh horizontal time constants selection 00 Slow; 01 Normal; 10 Reserved; 11 Fast
18	Foet_2fh	R/W	0x0	forced odd/even field toggle 0 toggles when signal interlaced; 1 interlaced - toggle each field in phase, non-interlaced = toggle each field random phase
17	Fsel_2fh	R/W	0x0	select 50/60Hz[0/1] if aufd_2fh=,Äô0,Äô
16	Aufd_2fh	R/W	0x1	0 select field freq. using fsel_2h; 1 automatic field detection
15:8	Hss_2fh	R/W	0xFB	horizontal sync output stop position
7:0	Hsb_2fh	R/W	0xFA	horizontal sync output begin position
Offset 0x148	***Subpix_2fhpllsync20***			
31:20	RSD_31To20	R	0x000	Reserved
19:10	Vsto_2fh	R/W	0x209	vertical sync stop position
9:0	Vsta_2fh	R/W	0x004	vertical sync start position
Offset 0x14C	***Subpix_2fhpllsync30***			
31:20	RSD_31To20	R	0x000	Reserved
19:10	Hrefs_2fh	R/W	0x037	horizontal href pulse stop position
9:0	Hrefb_2fh	R/W	0x3AD	horizontal href start position
Offset 0x180	***Dmsd_h_sync0***			
31:23	RSD_31To23	R	0x000	Reserved

Table 2: VIDDEC Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
22:21	Dmsd_atvt	R/W	0x1	tv/vcr detection threshold
20:19	Dmsd_hdel	R/W	0x0	Set delay of Horizontal Sync
18:11	Dmsd_hss	R/W	0xFB	Horizontal Sync Stop
10:3	Dmsd_hsb	R/W	0xFA	Horizontal Sync Begin
2:1	Dmsd_htc	R/W	0x1	Horizontal Time Constant
0	Dmsd_hpll	R/W	0x0	Horizontal PLL Control
Offset 0x184	***Dmsd_v_sync0***			
31:26	RSD_31To26	R	0x00	Reserved
25	Dmsd_vgps	R/W	0x0	Influences Field offset of Vertical Blanking (TBC)
24:16	Dmsd_vsto	R/W	0x12F	Vertical sync stop position
15:7	Dmsd_vsta	R/W	0x002	Vertical sync start position
6	Dmsd_foet	R/W	0x1	Forced Odd/Even Toggle
5	Dmsd_fsel	R/W	0x0	Field Length Select 0: 50Hz (nominal = 625 lines) 1: 60 Hz (nominal = 252 lines) Only effective if AUFD = 0
4	Dmsd_aufd	R/W	0x1	Automatic field length detection 0: off 1: active (recommended)
3	Dmsd_vnoi_max	R/W	0x0	Maximum vertical noise reduction
2	Dmsd_vnoi_rst	R/W	0x0	Vertical Noise reduction reset
1:0	Dmsd_vnoi	R/W	0x0	Vertical noise reduction mode
Offset 0x188	***Dmsd_std_det0***			
31:19	RSD_31To19	R	0x0000	Reserved
18	Dmsd_fscq	R/W	0x0	Fast PAL/SECAM sequence correction enable
17	Dmsd_colo	R/W	0x0	Force colour on
16:13	Dmsd_sthr	R/W	0x9	Colour Kill level for SECAM
12:9	Dmsd_qthr	R/W	0x9	Colour Kill level for PAL/NTSC
8:6	Dmsd_latency	R/W	0x3	Latency for Automatic Standart Detection
5:3	Dmsd_cstd	R/W	0x0	color standard selection 50 Hz / 60 Hz
2	Dmsd_auto_short	R/W	0x0	Automatic TV system Detection short loop
1:0	Dmsd_auto	R/W	0x2	Automatic TV system Detection
Offset 0x18C	***Dmsd_col_dec0***			
31:24	RSD_31To24	R	0x00	Reserved
23:20	Dmsd_idel	R/W	0x7	Horizontal Incremental delay
19	Dmsd_acl_on	R/W	0x1	Automatic Colour Limitter
18	Dmsd_fctc	R/W	0x0	Fast Chroma PLLTime Constant.
17:11	Dmsd_cgain	R/W	0x00	Chroma Gain Value
10	Dmsd_acgc	R/W	0x0	Automatic Chroma Gain Control
9	Dmsd_dccf	R/W	0x0	Disable PAL delay line
8:1	Dmsd_huec	R/W	0x00	Hue Control
0	Dmsd_cdto	R/W	0x0	Clear Chrominance DTO.

Table 2: VIDDEC Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
Offset 0x190	***Dmsd_filters0***			
31:26	RSD_31To26	R	0x00	Reserved
25:24	Dmsd_vedt	R/W	0x1	Comb filter, Vertical difference threshold
23:22	Dmsd_cmbt	R/W	0x1	Comb filter, comb amplitude threshold
21:20	Dmsd_hodg	R/W	0x2	Comb filter, Horizontal difference gain
19:18	Dmsd_vedg	R/W	0x2	Comb filter, vertical difference gain
17:16	Dmsd_medg	R/W	0x2	Comb filter, Median gain
15	Dmsd_byps	R/W	0x0	Bypass Chroma trap / Ycomb
14	Dmsd_ldel	R/W	0x0	Delay correction in NON-comb filter mode
13:11	Dmsd_ydel	R/W	0x0	Luminance Delay (WRT Chroma)
10:7	Dmsd_lufi	R/W	0x0	Luminance Peaking
6	Dmsd_ccomb	R/W	0x1	Activate Adaptive CComb
5	Dmsd_ycomb	R/W	0x1	Activate Adaptive YComb
4	Dmsd_lubw	R/W	0x0	Luminance Bandwidth
3	Dmsd_chbw	R/W	0x0	Chroma Bandwidth
2:0	Dmsd_lcbw	R/W	0x6	Luma/Chroma Bandwidth
Offset 0x194	***Dmsd_outputs0***			
31:30	RSD_31To30	R	0x0	Reserved
29	Dmsd_dither	R/W	0x0	dithering of 10th output bit for FEF
28	Dmsd_ofts3	R/W	0x1	its_combdec noiseshaping ('1'=OFF)
27:20	Dmsd_satn	R/W	0x40	Chrominance Saturation control
19:12	Dmsd_brig	R/W	0x80	Luminance Brightness control
11:4	Ddmsd_cont	R/W	0x44	Luminance Contrast control
3:2	Dmsd_voff	R/W	0x0	V (RMY) offset
1:0	Dmsd_uoff	R/W	0x0	U (BMY) offset
Offset 0x198	***Dmsd_misc0***			
31:21	RSD_31To21	R	0x000	Reserved
20	Dmsd_set_vbi	R/W	0x0	Bypass luminance and chrominance filtering during VBI
19:12	Dmsd_rawo	R/W	0x00	Luminance Gain for RAW data mode
11:4	Dmsd_rawg	R/W	0x00	Luminance Offset for RAW data mode
3	Dmsd_set_raw	R/W	0x0	Raw data mode
2	Dmsd_cm99	R/W	0x0	Compatibiltiy with 7199 Encoder
1:0	Dmsd_xsel	R/W	0x2	Crystal frequency select
Offset 0x300	***Dtm_mstab0***			
31:2	RSD_31To2	R	0x00000000	Reserved
1:0	Dtm_m_stab	R/W	0x0	
Offset 0x304	***Mtd_mstab0***			
31:2	RSD_31To2	R	0x00000000	Reserved

Table 2: VIDDEC Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
1:0	Mtd_m_stab	R/W	0x0	
Offset 0x308	***Copy_buffer0***			
31:1	RSD_31To1	R	0x00000000	Reserved
0	Copy_buffers	W	0x0	software copy to buffer command overruling vsync
Offset 0xFCC	***Debugctrl0***			
31:8	RSD_31To8	R	0x000000	Reserved
7:0	Debugcontrol	R/W	0x00	low latency,moved to csn_dtl2viddec
Offset 0xFE0	***Viddec_int_cond0***			
31:23	RSD_31To23	R	0x000	Reserved
22	Ics_dmsd_nfld	R	0x0	input signal field length detection changed
21	Ics_dmsd_tvdet	R	0x0	input signal time base detection changed
20	Ics_fastblank_in2	R	0x0	detected level at fastblank input 2 changed
19	Ics_fastblank_in1	R	0x0	detected level at fastblank input 1 changed
18	Ics_dto_atsc	R	0x0	2fh pll atsc detection status changed
17	Ics_2fhpll_fidt	R	0x0	field frequency detected by 2fh loop changed
16	Ics_dtc_tdc_lock	R	0x0	dtc_tdc_lock status (digital) changed
15	Ics_dll_lock	R	0x0	dtc_tdc_lock status (analogue) changed
14	Ics_agc_y_cyc_gain_limit	R	0x0	gain of Ycrcb AGC hardware loop tries to exceed limit
13	Ics_agc_cvbs_yc_gain_limit	R	0x0	gain of CVBS&Yyc AGC hardware loop tries to exceed limit
12	Ics_agc_sync_gain_limit	R	0x0	gain of SYNC AGC hardware loop tries to exceed limit
11	Ics_2fhpll_hnoise	R	0x0	2FH horizontal noise detector status changed
10	Ics_2fhpll_interlaced	R	0x0	2FH interlaced changed
9	Ics_2fhpll_vlock	R	0x0	2FH vertical lock changed
8	Ics_2fhpll_hlock	R	0x0	2FH horizontal lock changed
7	Ics_dmsd_hnoise	R	0x0	1FH horizontal noise changed
6	Ics_dmsd_ftvs	R	0x0	1FH TV system changed
5	Ics_dmsd_copro	R	0x0	1FH horizontal lock changed
4	Ics_dmsd_code	R	0x0	1FH colour dection changed
3	Ics_dmsd_fidt	R	0x0	1FH field frequency changed
2	Ics_dmsd_intl	R	0x0	1FH interlaced changed
1	Ics_dmsd_vl	R	0x0	1FH vertical lock changed
0	Ics_dmsd_hl	R	0x0	1FH horizontal lock changed
Offset 0xFE4	***Viddec_irq_enab0***			
31:23	RSD_31To23	R	0x000	Reserved
22	Int_ena_dmsd_nfld	R/W	0x0	input signal field length detection
21	Int_ena_dmsd_tvdet	R/W	0x0	input signal time base detection
20	Int_ena_fastblank_in2	R/W	0x0	detected level at fastblank input 2

Table 2: VIDDEC Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
19	Int_ena_fastblank_in1	R/W	0x0	detected level at fastblank input 1
18	Int_ena_dto_atsc	R/W	0x0	2fh pll atsc detection status
17	Int_ena_2fhpll_fidt	R/W	0x0	field frequency detected by 2fh loop
16	Int_ena_dtc_tdc_lock	R/W	0x0	dtc_tdc_lock status (digital)
15	Int_ena_dll_lock	R/W	0x0	dtc_tdc_lock status (analogue)
14	Int_ena_agc_y_cyc_gain_limit	R/W	0x0	gain of Ycrcb AGC hardware loop tries to exceed limit
13	Int_ena_agc_cvbs_yc_gain_limit	R/W	0x0	gain of CVBS&Yyc AGC hardware loop tries to exceed limit
12	Int_ena_agc_sync_gain_limit	R/W	0x0	gain of SYNC AGC hardware loop tries to exceed limit
11	Int_ena_2fhpll_hnoise	R/W	0x0	2FH horizontal noise detector status
10	Int_ena_2fhpll_interlaced	R/W	0x0	2FH interlaced
9	Int_ena_2fhpll_vlock	R/W	0x0	2FH vertical lock
8	Int_ena_2fhpll_hlock	R/W	0x0	2FH horizontal lock
7	Int_ena_dmsd_hnoise	R/W	0x0	1FH horizontal noise
6	Int_ena_dmsd_ftvs	R/W	0x0	1FH TV system
5	Int_ena_dmsd_copro	R/W	0x0	1FH horizontal lock
4	Int_ena_dmsd_code	R/W	0x0	1FH colour dection
3	Int_ena_dmsd_fidt	R/W	0x0	1FH field frequency
2	Int_ena_dmsd_intl	R/W	0x0	1FH interlaced
1	Int_ena_dmsd_vl	R/W	0x0	1FH vertical lock
0	Int_ena_dmsd_hl	R/W	0x0	1FH horizontal lock
Offset 0xFE8	***Viddec_irq_clr0***			
31:23	RSD_31To23	R	0x000	Reserved
22	Int_clr_dmsd_nfld	W	0x0	input signal field length detection
21	Int_clr_dmsd_tvdet	W	0x0	input signal time base detection
20	Int_clr_fastblank_in2	W	0x0	detected level at fastblank input 2
19	Int_clr_fastblank_in1	W	0x0	detected level at fastblank input 1
18	Int_clr_dto_atsc	W	0x0	2fh pll atsc detection status
17	Int_clr_2fhpll_fidt	W	0x0	field frequency detected by 2fh loop
16	Int_clr_dtc_tdc_lock	W	0x0	dtc_tdc_lock status (digital)
15	Int_clr_dll_lock	W	0x0	dtc_tdc_lock status (analogue)
14	Int_clr_agc_y_cyc_gain_limit	W	0x0	gain of Ycrcb AGC hardware loop tries to exceed limit
13	Int_clr_agc_cvbs_yc_gain_limit	W	0x0	gain of CVBS&Yyc AGC hardware loop tries to exceed limit
12	Int_clr_agc_sync_gain_limit	W	0x0	gain of SYNC AGC hardware loop tries to exceed limit

Table 2: VIDDEC Registers *...Continued*

Bit	Symbol	Access	Reset Value	Description
11	Int_clr_2fhpll_hnoise	W	0x0	2FH horizontal noise detector status
10	Int_clr_2fhpll_interlaced	W	0x0	2FH interlaced
9	Int_clr_2fhpll_vlock	W	0x0	2FH vertical lock
8	Int_clr_2fhpll_hlock	W	0x0	2FH horizontal lock
7	Int_clr_dmsd_hnoise	W	0x0	1FH horizontal noise
6	Int_clr_dmsd_ftvs	W	0x0	1FH TV system
5	Int_clr_dmsd_copro	W	0x0	1FH horizontal lock
4	Int_clr_dmsd_code	W	0x0	1FH colour dection
3	Int_clr_dmsd_fidt	W	0x0	1FH field frequency
2	Int_clr_dmsd_intl	W	0x0	1FH interlaced
1	Int_clr_dmsd_vl	W	0x0	1FH vertical lock
0	Int_clr_dmsd_hl	W	0x0	1FH horizontal lock
Offset 0xFEC	***Viddec_irq_set0***			
31:23	RSD_31To23	R	0x000	Reserved
22	Int_set_dmsd_nfld	W	0x0	input signal field length detection
21	Int_set_dmsd_tvdet	W	0x0	input signal time base detection
20	Int_set_fastblank_in2	W	0x0	detected level at fastblank input 2
19	Int_set_fastblank_in1	W	0x0	detected level at fastblank input 1
18	Int_set_dto_atsc	W	0x0	2fh pll atsc detection status
17	Int_set_2fhpll_fidt	W	0x0	field frequency detected by 2fh loop
16	Int_set_dtc_tdc_lock	W	0x0	dtc_tdc_lock status (digital)
15	Int_set_dll_lock	W	0x0	dtc_tdc_lock status (analogue)
14	Int_set_agc_y_cyc_gain_limit	W	0x0	gain of Ycrcb AGC hardware loop tries to exceed limit
13	Int_set_agc_cvbs_yc_gain_limit	W	0x0	gain of CVBS&Yyc AGC hardware loop tries to exceed limit
12	Int_set_agc_sync_gain_limit	W	0x0	gain of SYNC AGC hardware loop tries to exceed limit
11	Int_set_2fhpll_hnoise	W	0x0	2FH horizontal noise detector status
10	Int_set_2fhpll_interlaced	W	0x0	2FH interlaced
9	Int_set_2fhpll_vlock	W	0x0	2FH vertical lock
8	Int_set_2fhpll_hlock	W	0x0	2FH horizontal lock
7	Int_set_dmsd_hnoise	W	0x0	1FH horizontal noise
6	Int_set_dmsd_ftvs	W	0x0	1FH TV system
5	Int_set_dmsd_copro	W	0x0	1FH horizontal lock
4	Int_set_dmsd_code	W	0x0	1FH colour dection
3	Int_set_dmsd_fidt	W	0x0	1FH field frequency
2	Int_set_dmsd_intl	W	0x0	1FH interlaced
1	Int_set_dmsd_vl	W	0x0	1FH vertical lock

Table 2: VIDDEC Registers *…Continued*

Bit	Symbol	Access	Reset Value	Description
0	Int_set_dmsd_hl	W	0x0	1FH horizontal lock
Offset 0xFFC	***Viddec_id0***			
31:16	Id	R	0x0140	Module identifier.
15:12	Major_revision	R	0x2	Major revision. Any revisions that may break software compatibility.
11:8	Minor_revision	R	0x0	Minor revision. Any revisions that still keep software compatibility.
7:0	Aperture_size	R	0x00	Aperture size. Encoded as (aperture size/4K)-1; so 0 means 4K (the default).

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